

Model Name: B460M DS3H AC

SHEET

TITLE

Rev 1.1

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B-DDR4
06	CPU_LGA1151-C
07	CPU_LGA1150-D
08	DDR4 CHANNEL A
09	DDR4 CHANNEL B
10	PCH_CLK BUFFER
11	PCH_DMI,USB,PCIE
12	PCH_MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH PWR
15	PCH GND
16	ITE 8686 LPC IO
17	HWM
18	FAN CTRL--SIO
19	BIOS
20	CEC
21	PCI EXPRESS*16 SLOT
22	PCI EXPRESS*1 SLOT
23	SATA Connector
24	M.2 X4 (A)
25	IT8892E (NA)
26	PCI SLOT (NA)
27	ASM1085 POWER (NA)
28	LDO POWER (NA)

SHEET

TITLE

29	ISL95866 PWM-IRON
30	ISL95866 VCORE-IRON
31	ISL95866 VCCGT-IRON
32	VCCSA_VCCIO_VCCPLL
33	RT8237_DDR_BEAD
34	RT8068A_VPP
35	RT8237_PCH-BEAD
36	DISCRETE POWER
37	POWER MAP
38	ATX POWER , A_-PROCHOT
39	KB_MS
40	DVI CONN
41	RTD2168 - DP to VGA - IC
42	RTD2168 - DP to VGA - Conn
43	REALTEK 8111G
44	USB_LAN CONNECTOR-81118
45	Realtek ALC887
46	REAR AUDIO JACK
47	ADUIO LED
48	R_USB30_1
49	R_USB30_2
50	HDMI (MASK)
51	Redriver-R_USB31 (NA)
52	F_USB30
53	F_USB
54	F_PANEL
55	COM, TPM
56	EMI-ESD
	NTC MAP

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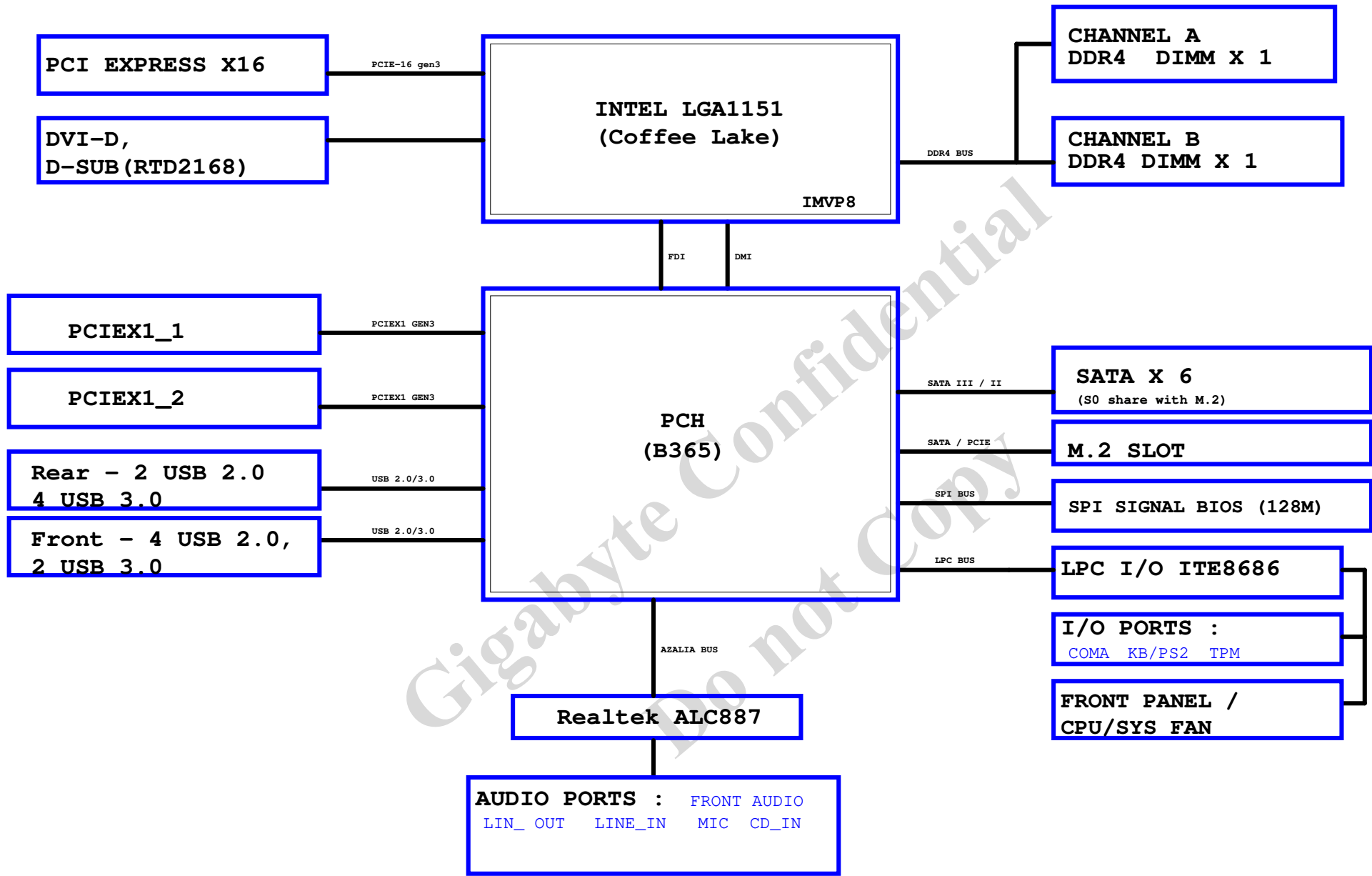
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Size	Document Number	B460M DS3H AC	
Custom		Rev	1.1
Date:	Monday, August 31, 2020	Sheet	1 of 63

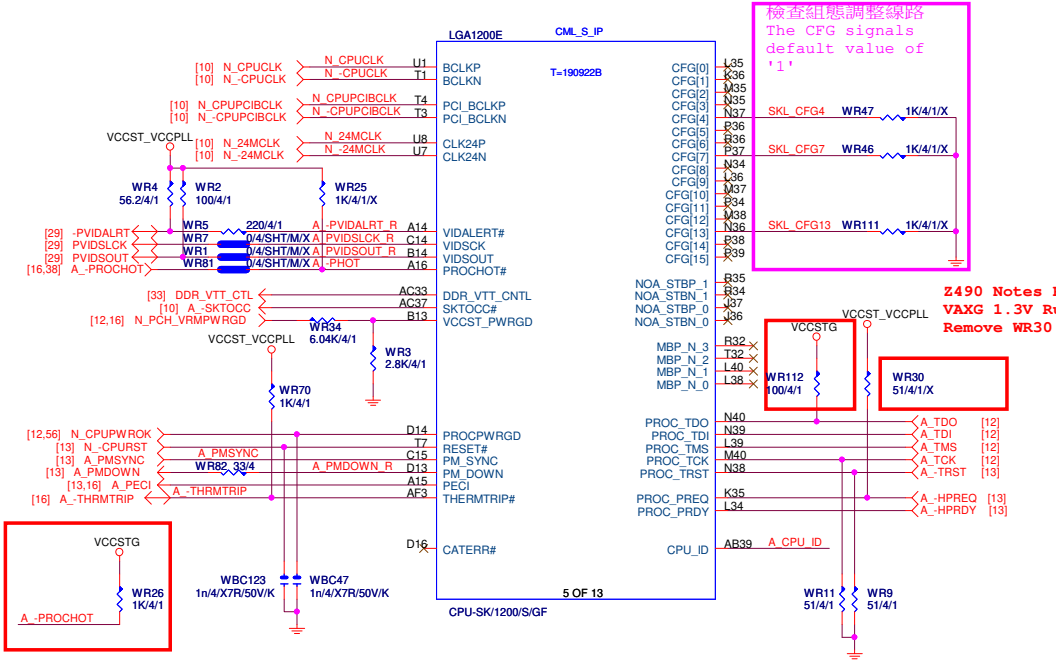
Circuit or PCB layout change

2020/03/17

DATE	Change Item	Reason
2020/03/17	Update to R1.01 Update HDA_SDO 線路 [P12] Update CHA&B DDR Vref	

BLOCK DIAGRAM

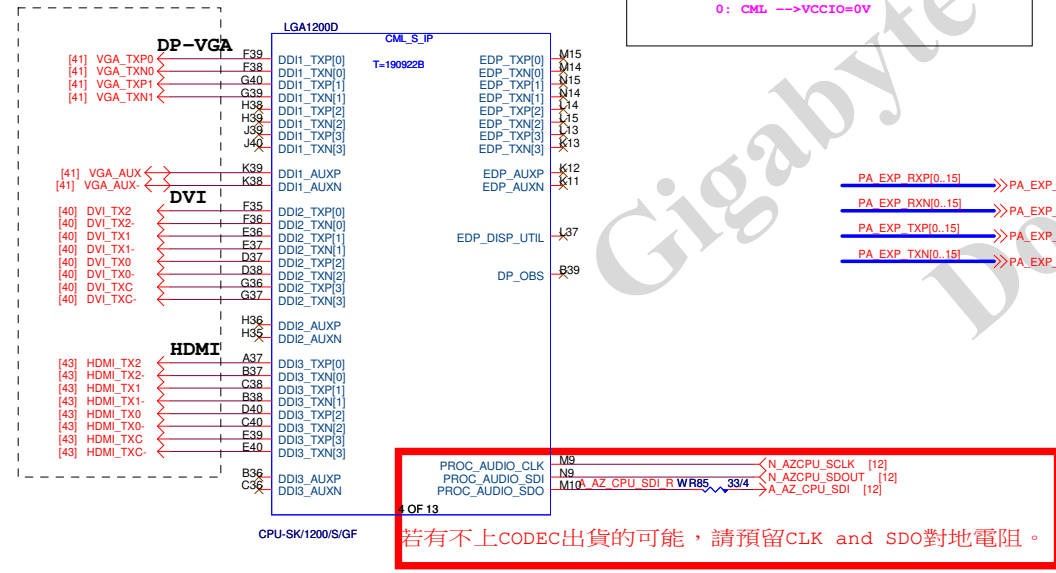
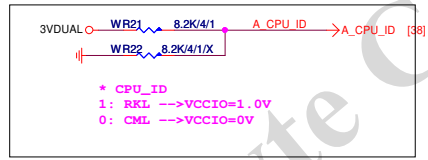




檢查組態調整線路
The CFG signals
default value of
'1'

CFG[4]: 0=eDP enable / 1=eDP disable
CFG[7]: 1=PEG Train immediately following RESET
0=PEG Wait for BIOS
CFG[13]: 1=VCCSA Fixed Mode / 0=SVID Mode

Z490 Notes Rev 1.05
VAXG 1.3V Run PTU VAXG High & CPU OC 5G hang issue
Remove WR30



若有不上CODEC出貨的可能，請預留CLK and SDO對地電阻。

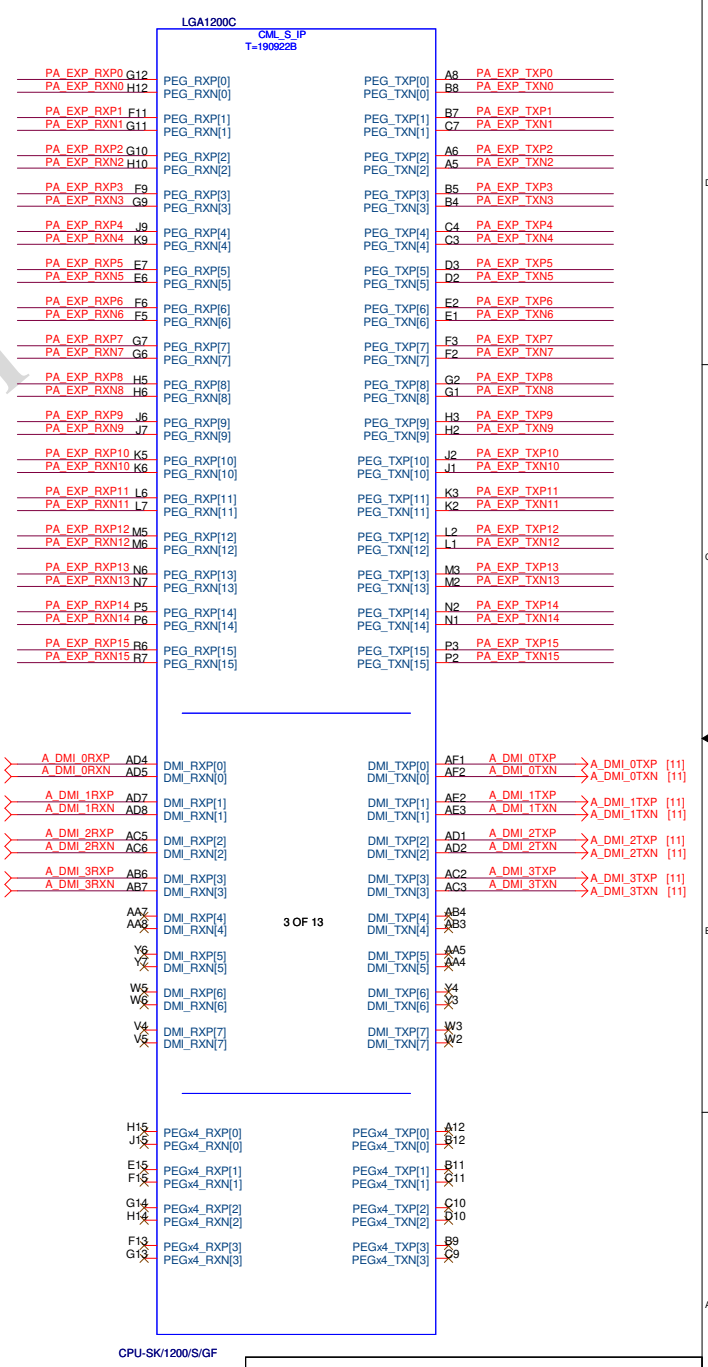
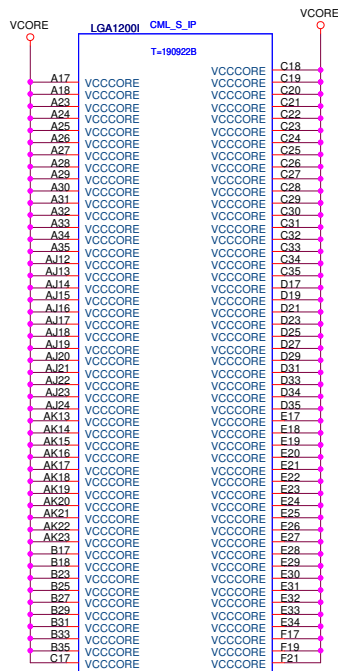
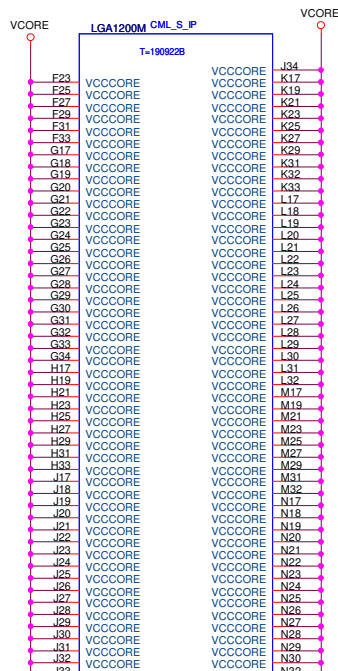


Figure 1 displays a comparison of the proposed method (left column) and existing methods (right column) across four datasets: MODT_A, MODT_B, MDA, and MDB. Each row shows the distribution of the proposed method (blue line) and the existing methods (red line). The x-axis represents the value of the variable, and the y-axis represents the density. The proposed method consistently shows a more accurate and stable distribution compared to the existing methods.



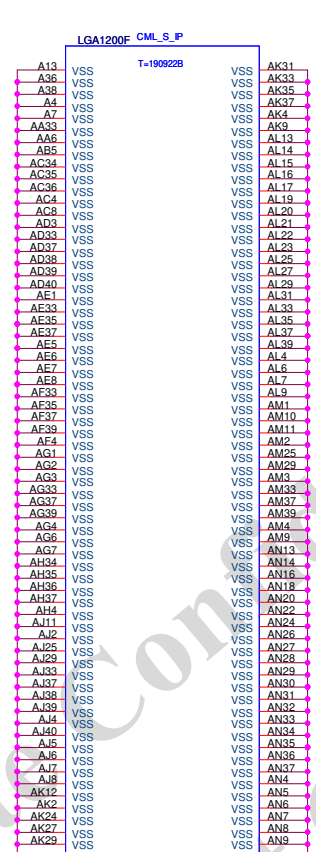
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CPU-SK/1200/S/GF



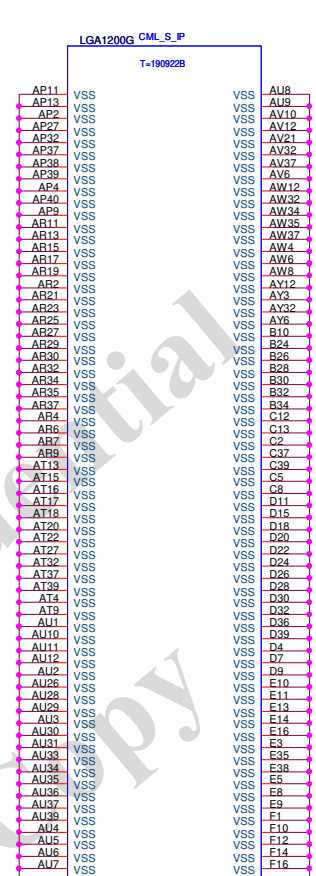
VCCORE_SENSE
SSCORE_SENSE

10 OF 13
CPU-SK/1200/S/GF



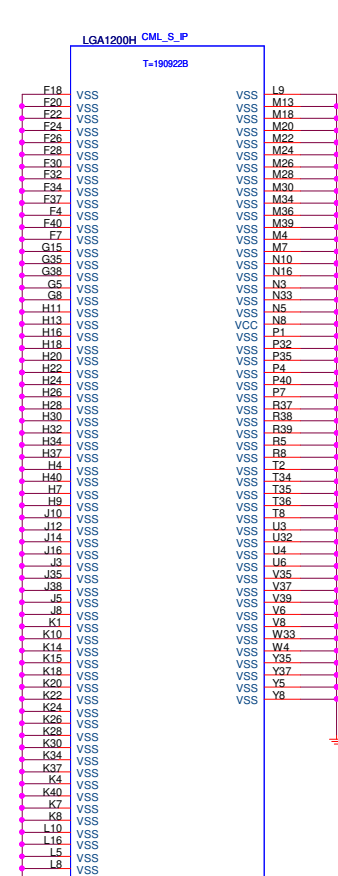
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CPU-SK/1200/S/GF



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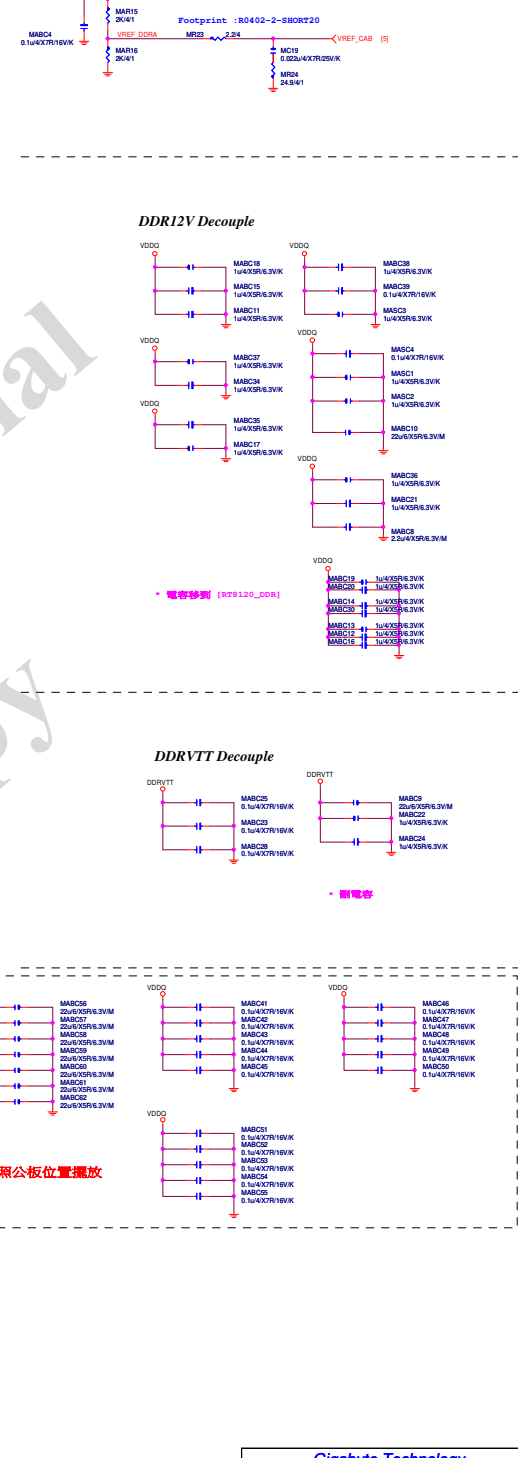
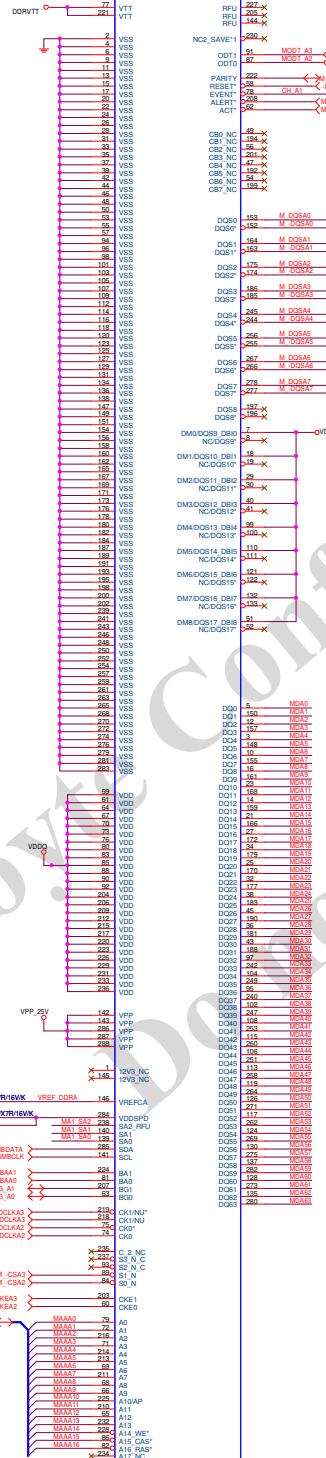
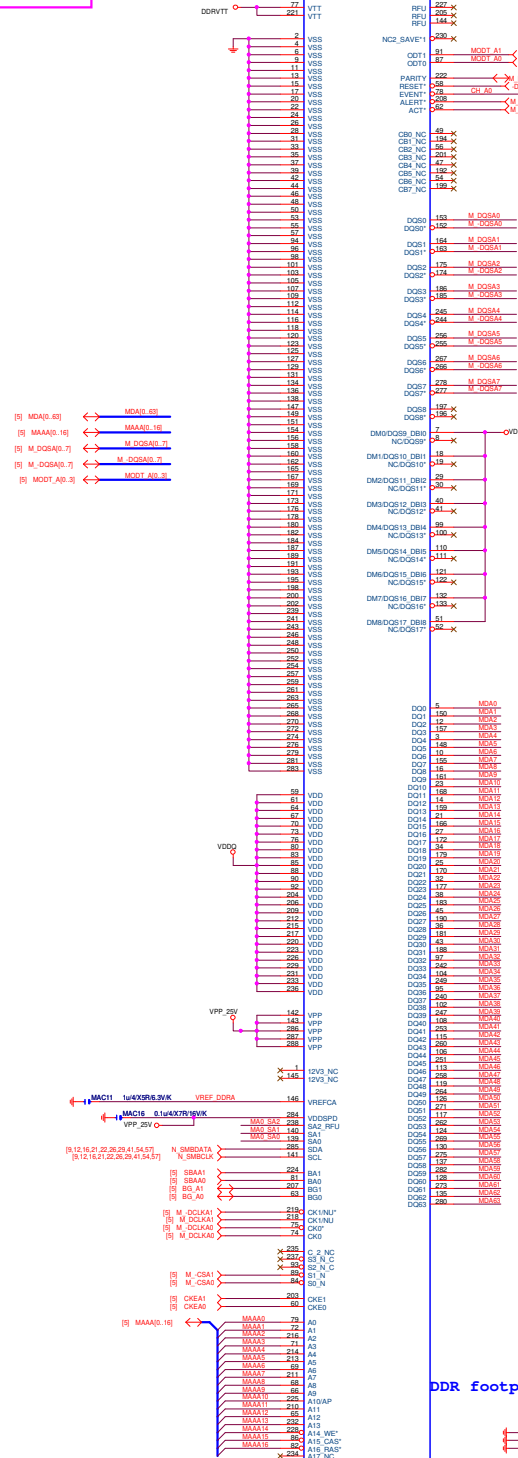
CPU-SK/1200/S/GF

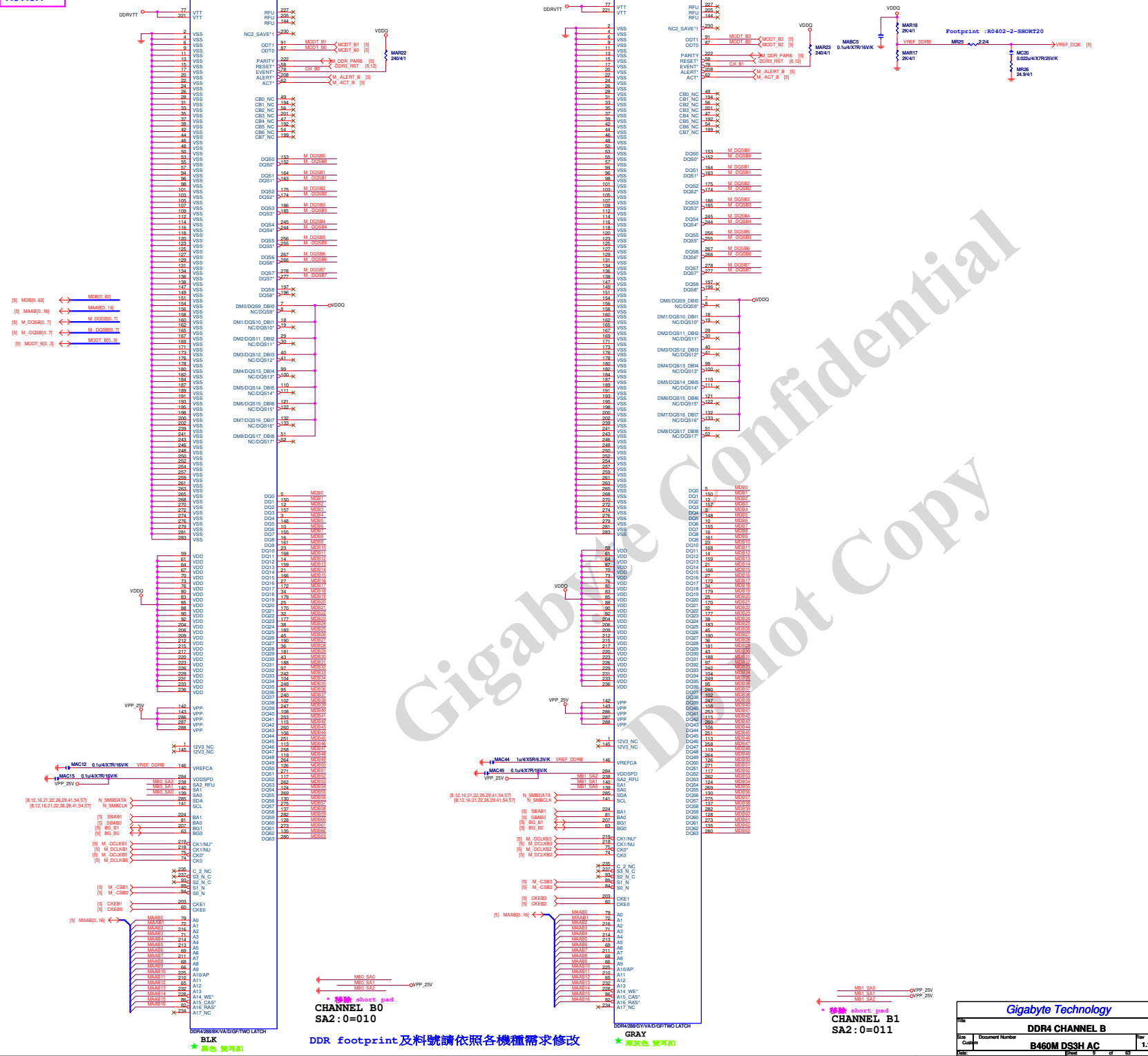


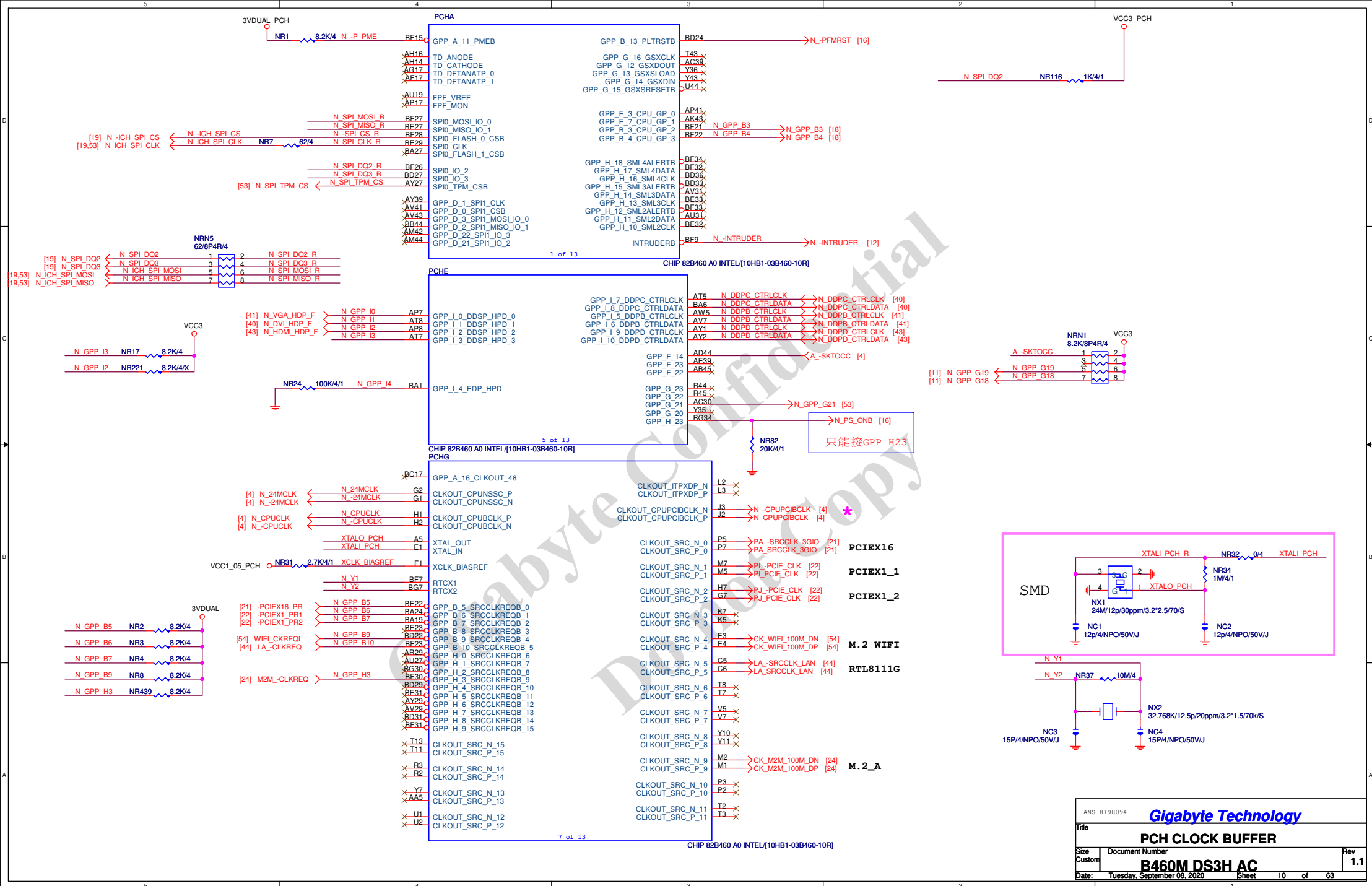
8 OF 13

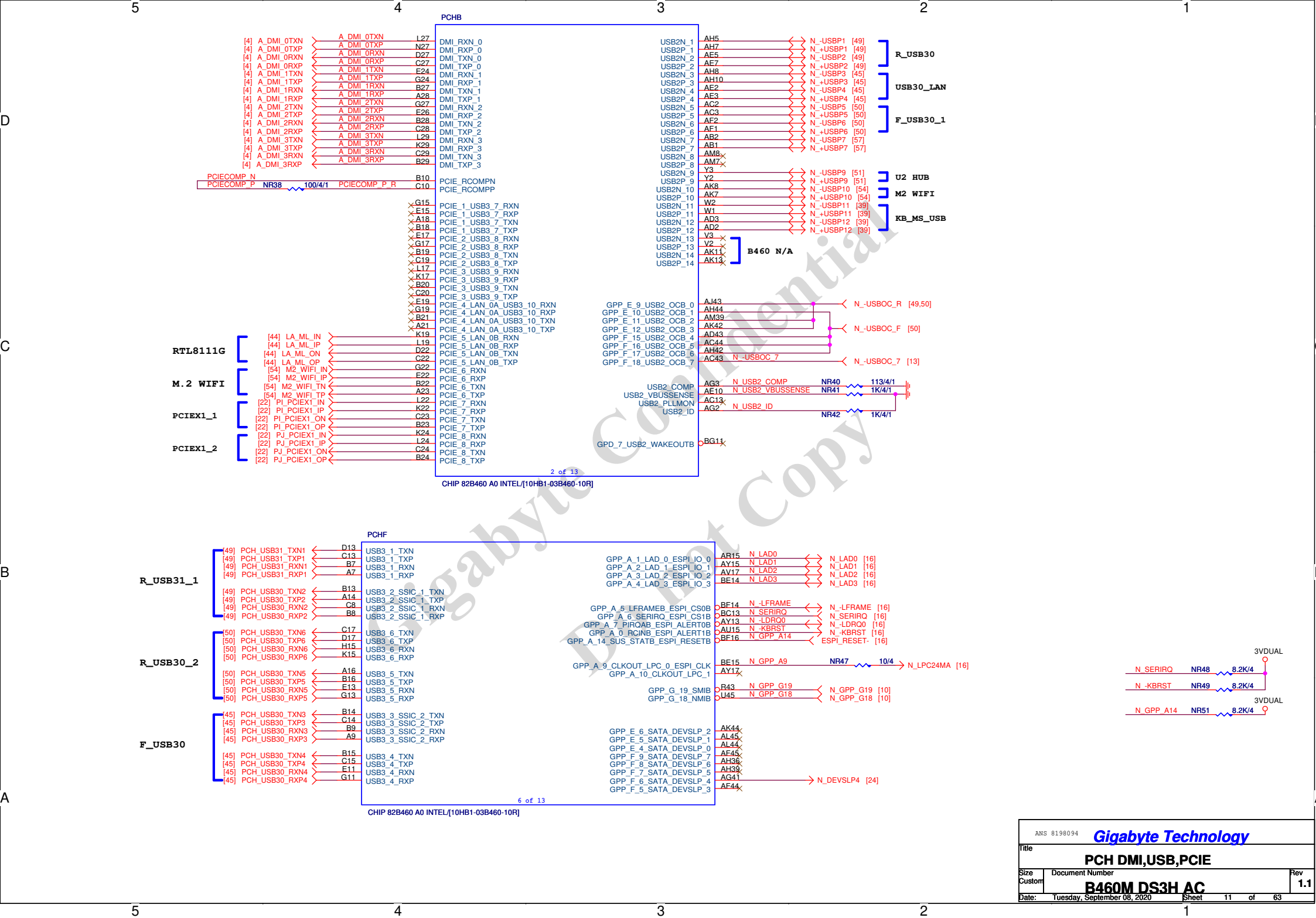
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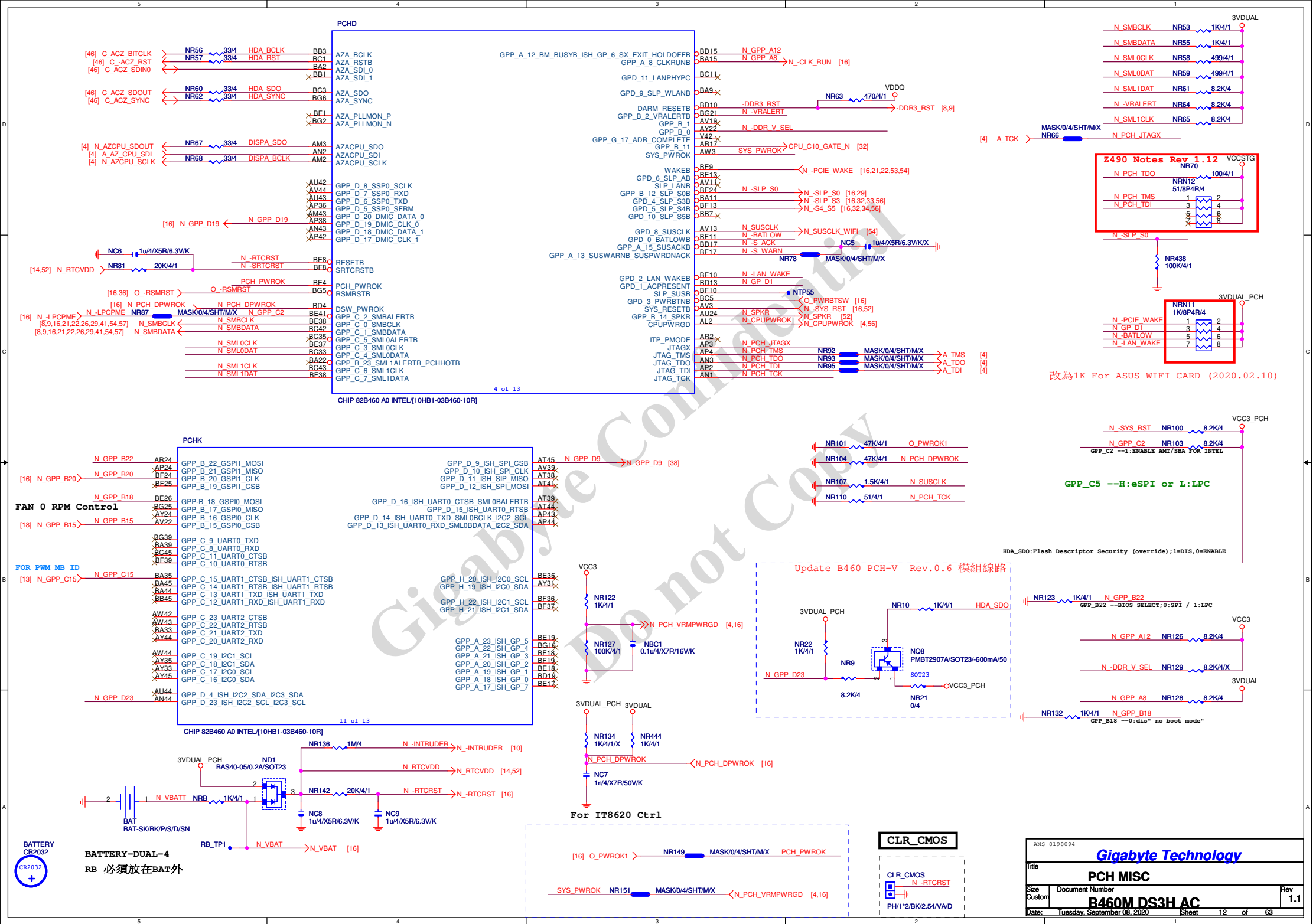
* 刪 Vcore 電容











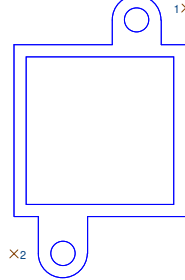
PCHI		
A25	VSS	A42
A30	VSS	D45
P22	VSS	BG44
AV38	VSS	BF44
AV45	VSS	BF45
AV8	VSS	BF2
AY11	VSS	W29
AY19	VSS	A35
AY37	VSS	A40
AY4	VSS	A41
AY42	VSS	AA17
AY8	VSS	AA18
B25	VSS	AA20
B3	VSS	AA21
B30	VSS	AA26
B35	VSS	AA28
B4	VSS	AA29
B41	VSS	AB17
BA13	VSS	AC32
BA17	VSS	AE4
BA25	VSS	AE8
BA31	VSS	AF18
BA37	VSS	AF20
BA4	VSS	AF21
BA42	VSS	AF25
BB40	VSS	AF28
BC38	VSS	AF29
BC40	VSS	AF4
BC9	VSS	AF42
BD11	VSS	AG18
BD16	VSS	AG20
BD2	VSS	AG21
BD21	VSS	AG23
BD25	VSS	AG25
F2	VSS	AG26
E31	VSS	AG28
E6	VSS	AG29
E8	VSS	AH11
F39	VSS	AH13
F43	VSS	AH30
G4	VSS	AH32
G40	VSS	AH33
G42	VSS	AH38
F6	VSS	AJ1
G9	VSS	AJ17
H11	VSS	AJ18
H13	VSS	AJ20
H17	VSS	AJ21
H19	VSS	AJ23
H22	VSS	AJ25
H24	VSS	AJ26
H27	VSS	AJ28
H29	VSS	AJ29
H33	VSS	AJ45
H35	VSS	AK10
H38	VSS	AK14
H4	VSS	AK16
H42	VSS	AK17
H9	VSS	AK18
J4	VSS	AK26
M35	VSS	AK28
M38	VSS	AM14
M4	VSS	AN14
M8	VSS	AP19
M9	VSS	AR22
N13	VSS	AR27
N15	VSS	AU29
N19	VSS	AU33
N22	VSS	AV1
N24	VSS	AV10
N31	VSS	AV15
N42	VSS	AV24
P10	VSS	AV27
P12	VSS	AV33
AV35	VSS	

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CHIP 82B460 A0 INTEL[10HB1-03B460-10R]

PCHL		
BD34	VSS[70]	AB18
BD39	VSS[71]	AB20
BD7	VSS[72]	AB21
BE2	VSS[73]	AB25
BF43	VSS[74]	AB29
BF5	VSS[75]	AB4
BG18	VSS[76]	AB42
BG23	VSS[77]	AC10
BG28	VSS[78]	AC11
BG32	VSS[79]	AC14
BG37	VSS[80]	AC16
BG40	VSS[81]	AC38
BG9	VSS[83]	AC4
C1	VSS[84]	AC5
A12	VSS[85]	AC7
C2	VSS[86]	AC8
C37	VSS[87]	AD1
A6	VSS[88]	AD18
C9	VSS[89]	AD20
D1	VSS[90]	AD21
D10	VSS[91]	AD25
D12	VSS[92]	AD29
D15	VSS[93]	AD45
D16	VSS[94]	AE11
B12	VSS[95]	AE14
D19	VSS[96]	AE32
D21	VSS[97]	AE33
D24	VSS[98]	AE38
D25	VSS[99]	AK29
D29	VSS[100]	AK30
D30	VSS[101]	AK32
D33	VSS[102]	AK35
D35	VSS[103]	AK39
D36	VSS[104]	AL4
D39	VSS[105]	AL42
D44	VSS[106]	AM10
D7	VSS[107]	AM11
P13	VSS[108]	AM13
P15	VSS[109]	AM17
P17	VSS[110]	AM19
P19	VSS[111]	AM24
P21	VSS[112]	AM27
P33	VSS[113]	AM29
P35	VSS[114]	AM32
P4	VSS[115]	AM33
P42	VSS[116]	AM4
P8	VSS[117]	AN45
R1	VSS[118]	AP10
R32	VSS[119]	AP11
T10	VSS[120]	AP13
T14	VSS[121]	AP15
T22	VSS[122]	AP22
T29	VSS[123]	AP27
T32	VSS[124]	AP31
T36	VSS[125]	AP33
T38	VSS[126]	AP34
Y38	VSS[127]	AP39
Y4	VSS[128]	T4
Y8	VSS[129]	W26
T42	VSS[130]	W16
T5	VSS[131]	V17
U4	VSS[132]	V18
U42	VSS[133]	V30
V10	VSS[134]	V32
V14	VSS[135]	V33
W3	VSS[136]	V38
AR13	VSS[137]	V4
AR31	VSS[138]	V8
AR33	VSS[139]	
AR4	VSS[140]	W18
AT10	VSS[141]	W20
AT13	VSS[142]	W21
AT35	VSS[143]	W23
AT37	VSS[144]	W25
AT42	VSS[145]	
AU11	VSS[146]	A44
AU17	VSS[147]	BE1
BD30	VSS[148]	BD1
W45	VSS[149]	B1
Y13	VSS[150]	A2
Y14	VSS[151]	B2
Y30	VSS[152]	A3
Y32	VSS[153]	A4
Y33	VSS[154]	B44
Y34	VSS[155]	B45
BG14	VSS[156]	

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CHIP 82B460 A0 INTEL[10HB1-03B460-10R]

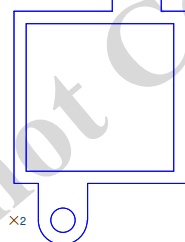
SB_HEATSIN



BGAHSINK_SB-42X42

PCH_HS
HEAT SINK/N-BG/GBT MK/H81/KWOG[12SP2-S04208-61R_12SP2-S04208-62R_12SP2-S04208-63R]

TMOS



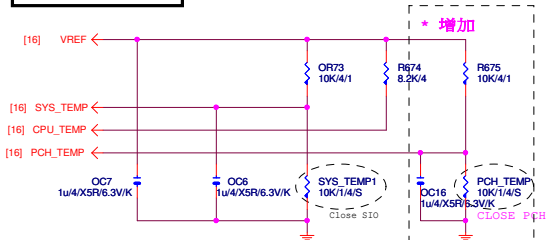
MOS_Heatsink[12SP2-S09425-11R_12SP2-S09425-12R]

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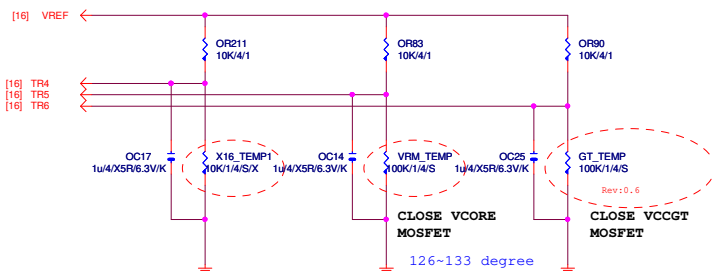
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Size	Document Number	Rev
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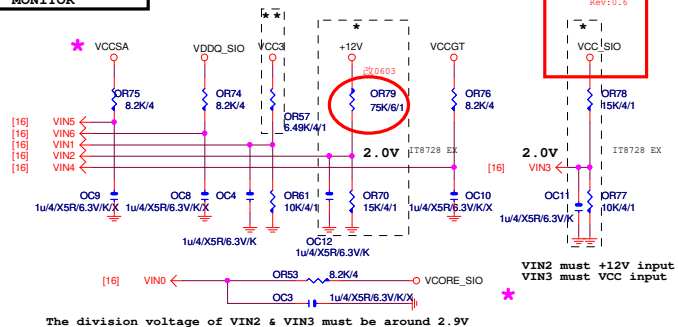
TEMP H/W MONITOR



低階機種: 3個FAN時使用

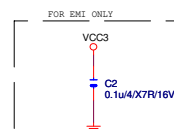
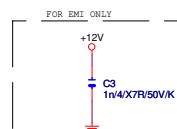


VOLTAGE-- H/W MONITOR



VCCBT PWF RS 0/6/SHT/30/X 03VDUAL_PCH

(靠近ATX CONNECTOR)



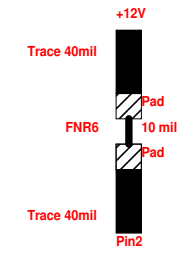
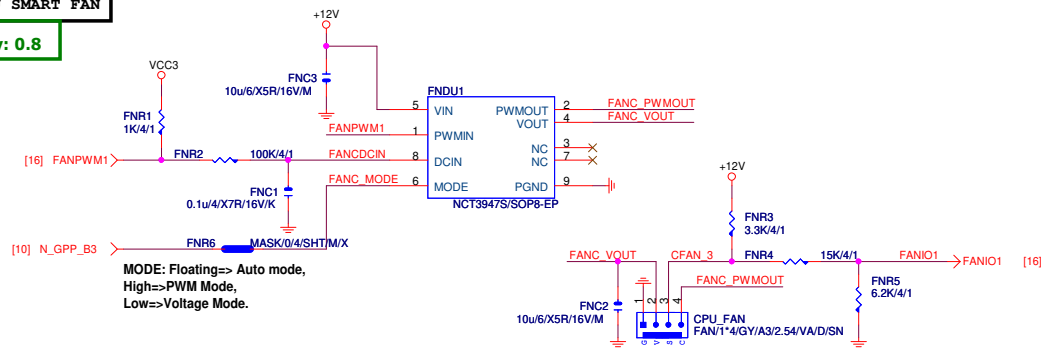
★Update 2015-04.24

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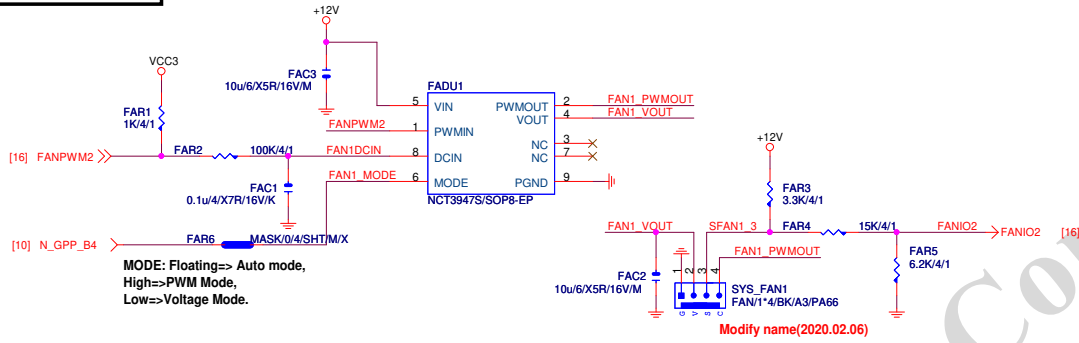
Title			HWM,KB/MS, FAN CTRL
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CPU SMART FAN

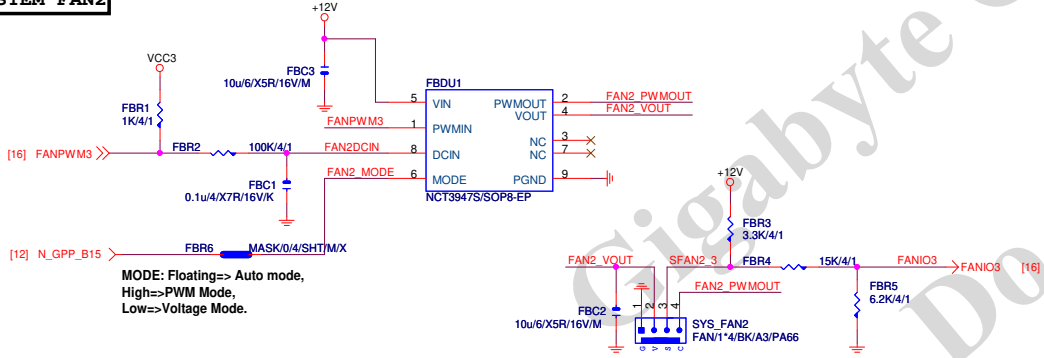
Rev: 0.8



A. SYSTEM FAN1



SYSTEM FAN2

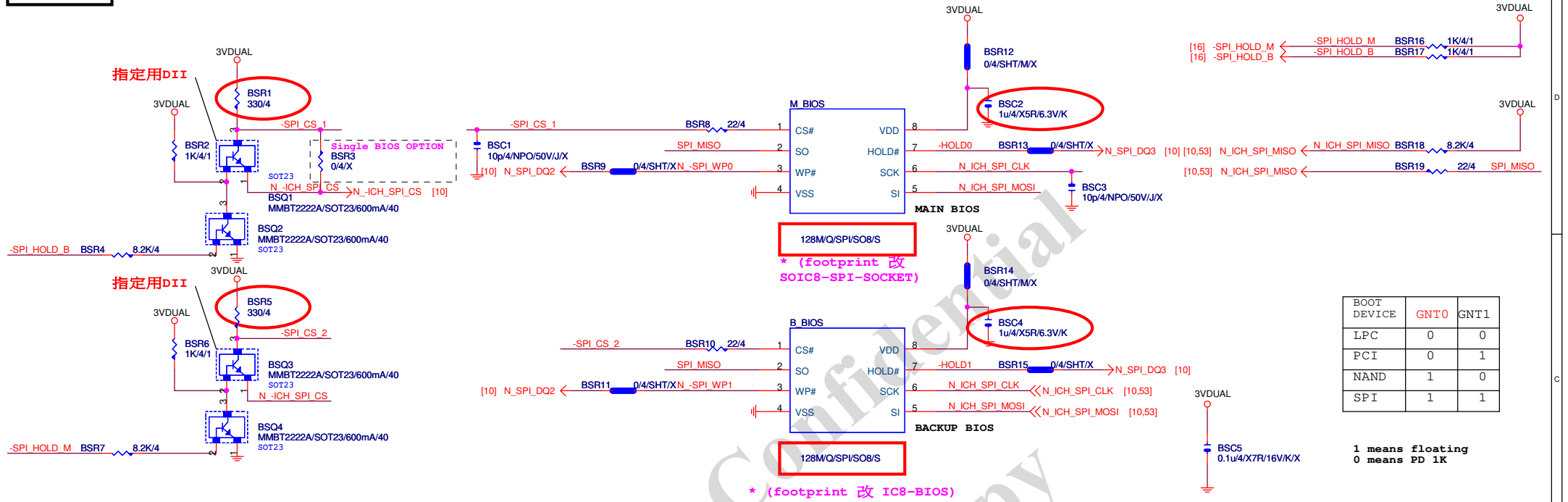


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Title			
FAN CTRL			
Size	Document Number	Rev	
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DUAL BIOS

MOSI For DMI RX Termination Voltage



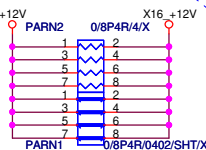
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BIOS			
File	BIOS		
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GIGABYTE™			
Title			
CEC relate circuit			
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+12 - protect
short-wire test



[8,9,12,16,22,26,29,41,54,57] N_SMBCLK
[8,9,12,16,22,26,29,41,54,57] N_SMBDATA

[12,16,22,53,54] N_-PCIE_WAKE

[10] -PCIE16_PR

PA_EXP_RXP0[0..15] >> PA_EXP_RXP[0..15] [4]
PA_EXP_RXN0[0..15] >> PA_EXP_RXN[0..15] [4]
PA_EXP_TXP0[0..15] >> PA_EXP_TXP[0..15] [4]
PA_EXP_TXN0[0..15] >> PA_EXP_TXN[0..15] [4]

PA_EXP_TXP0	PAC5	0.22u4/X5R6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u4/X5R6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u4/X5R6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u4/X5R6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u4/X5R6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u4/X5R6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u4/X5R6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u4/X5R6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u4/X5R6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u4/X5R6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u4/X5R6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u4/X5R6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u4/X5R6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u4/X5R6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u4/X5R6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u4/X5R6.3V/K	PA_EXP_TXN7_C
PA_EXP_TXP8	PAC21	0.22u4/X5R6.3V/K	PA_EXP_TXP8_C
PA_EXP_TXN8	PAC20	0.22u4/X5R6.3V/K	PA_EXP_TXN8_C
PA_EXP_TXP9	PAC22	0.22u4/X5R6.3V/K	PA_EXP_TXP9_C
PA_EXP_TXN9	PAC23	0.22u4/X5R6.3V/K	PA_EXP_TXN9_C
PA_EXP_TXP10	PAC24	0.22u4/X5R6.3V/K	PA_EXP_TXP10_C
PA_EXP_TXN10	PAC25	0.22u4/X5R6.3V/K	PA_EXP_TXN10_C
PA_EXP_TXP11	PAC26	0.22u4/X5R6.3V/K	PA_EXP_TXP11_C
PA_EXP_TXN11	PAC27	0.22u4/X5R6.3V/K	PA_EXP_TXN11_C
PA_EXP_TXP12	PAC28	0.22u4/X5R6.3V/K	PA_EXP_TXP12_C
PA_EXP_TXN12	PAC29	0.22u4/X5R6.3V/K	PA_EXP_TXN12_C
PA_EXP_TXP13	PAC30	0.22u4/X5R6.3V/K	PA_EXP_TXP13_C
PA_EXP_TXN13	PAC31	0.22u4/X5R6.3V/K	PA_EXP_TXN13_C
PA_EXP_TXP14	PAC32	0.22u4/X5R6.3V/K	PA_EXP_TXP14_C
PA_EXP_TXN14	PAC33	0.22u4/X5R6.3V/K	PA_EXP_TXN14_C
PA_EXP_TXP15	PAC34	0.22u4/X5R6.3V/K	PA_EXP_TXP15_C
PA_EXP_TXN15	PAC35	0.22u4/X5R6.3V/K	PA_EXP_TXN15_C

PA_EXP_TXP8_C

PA_EXP_TXN8_C

PA_EXP_TXP9_C

PA_EXP_TXN9_C

PA_EXP_TXP10_C

PA_EXP_TXN10_C

PA_EXP_TXP11_C

PA_EXP_TXN11_C

PA_EXP_TXP12_C

PA_EXP_TXN12_C

PA_EXP_TXP13_C

PA_EXP_TXN13_C

PA_EXP_TXP14_C

PA_EXP_TXN14_C

PA_EXP_TXP15_C

PA_EXP_TXN15_C

PCIEX16:16/5/5/5/16

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

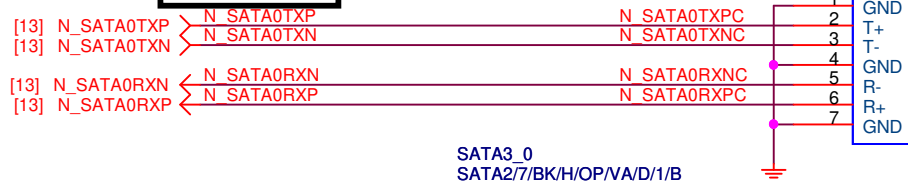
PCIESLOT-164P

PCIEX16 3GIO_*16

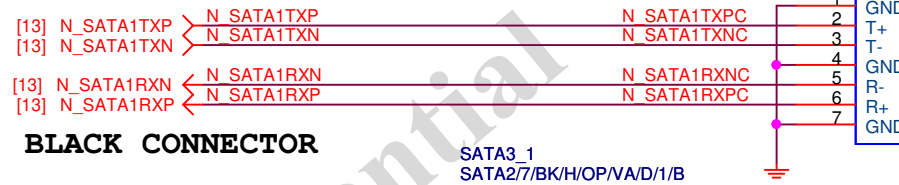
PCI-E/16X-164P/GY/LONG DOUBLE/HK/2

黑色SLOT

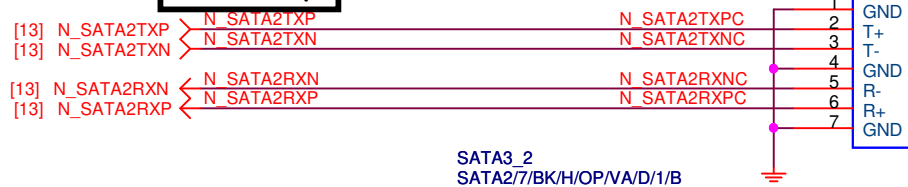
SATA3 0/1



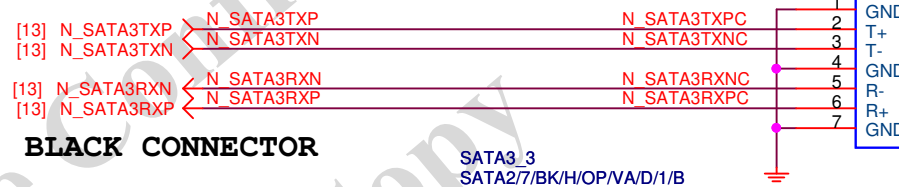
BLACK CONNECTOR



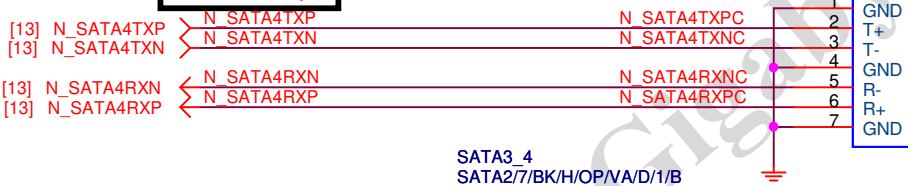
SATA3 2/3



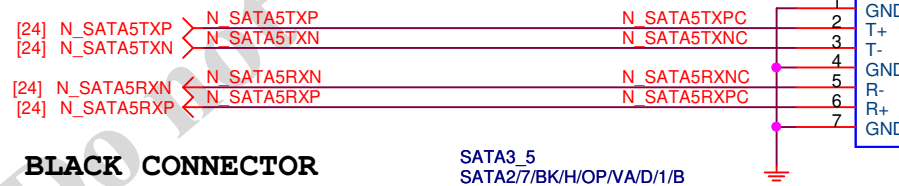
BLACK CONNECTOR



SATA3 4/5



BLACK CONNECTOR

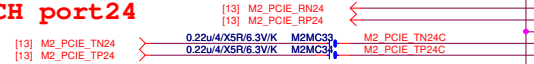


Gigabyte Technology

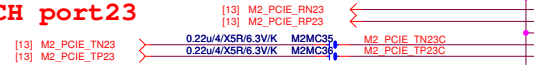
Title			SATA		
Size			Document Number		
Custom			B460M DS3H AC		
Date:			Monday, August 31, 2020	Sheet	23 of 63
				Rev	1.1

Rev 0.4

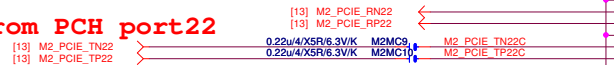
M.2 Lane4 from PCH port24



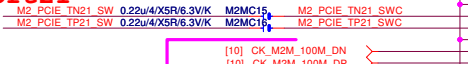
M.2 Lane3 from PCH port23



M.2 Lane2 from PCH port22



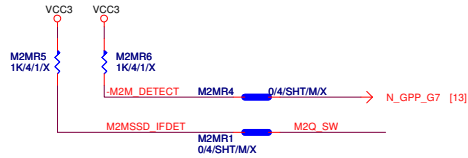
M.2 Lane2 from PCH port21



需與M2_-CLKREQ對應

SATA : GND.
PCIe : HIGH

支援SATA and M.2 function



* Footprint : m2_80_h2mm8w

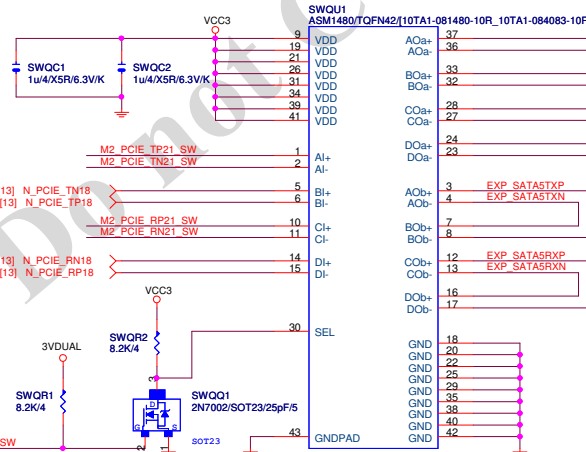
舊的Switch,價格低

SATA Conn

M2Q_SW

High : M2X4 + SATA 5 OK

Low : M2 (SATA) + SATA 5 NA



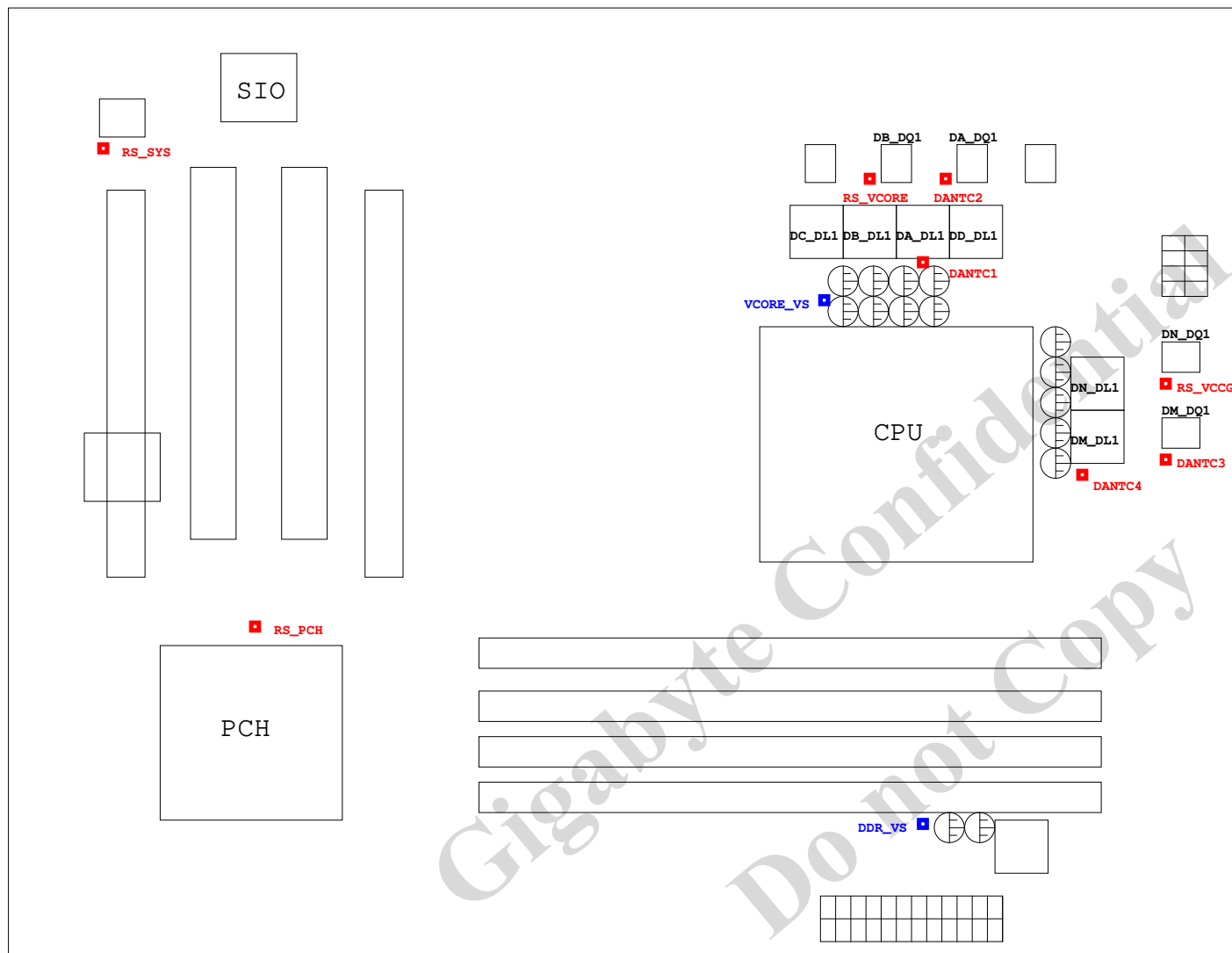
M.2 PCIE Mode

M.2 SATA Mode

Function	SEL
xI--> xOa	L
xI--> xOb	H

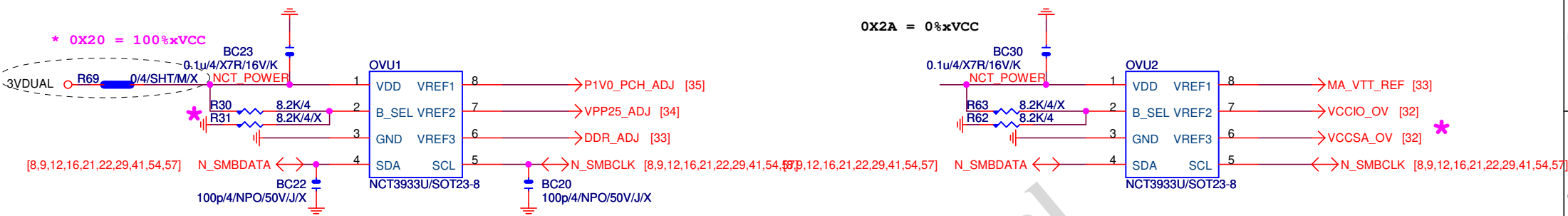
Gigabyte Technology

Title		
M.2 X4		
Size	Document Number	Rev
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Date:	Monday, August 31, 2020	Sheet 24 of 63



熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL1	N/A
DANTC2	DA_DQ1	Differential
DANTC3	DM_DQ1	N/A
DANTC4	DM_DL1	Differential
RS_VCORE	DB_DQ1	N/A
RS_VCCGT	DN_DQ1	N/A
RS_PCH	PCH	N/A
RS_SYS	CU1	N/A

OVER VOLTAGE



0X2A = 0%xVCC

0X22 = 75%xVCC

* 删除 ovu3

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology

TitleCPU CORE VR-2

Size Custom

Document Number

Rev1.1

Date: Monday, August 31, 2020

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REV: 0.1

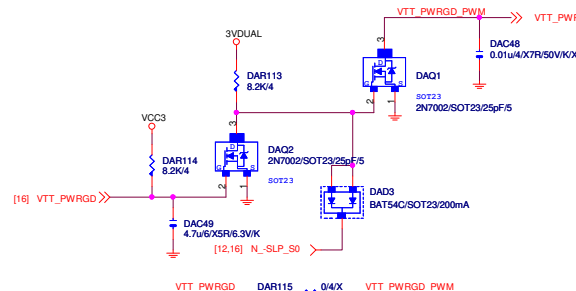
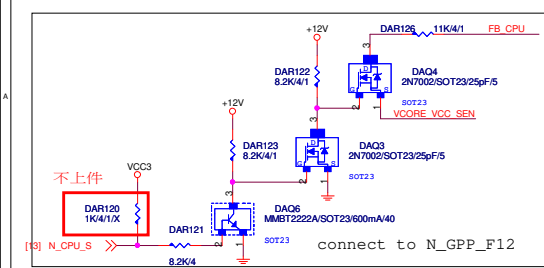
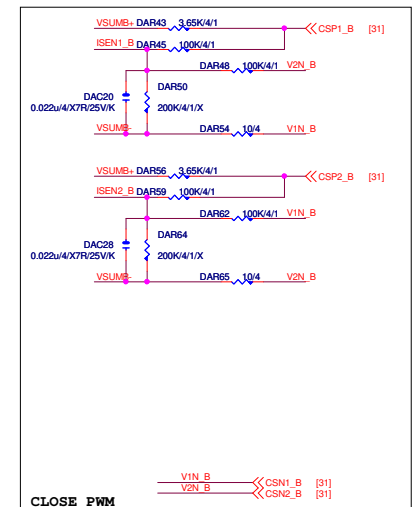
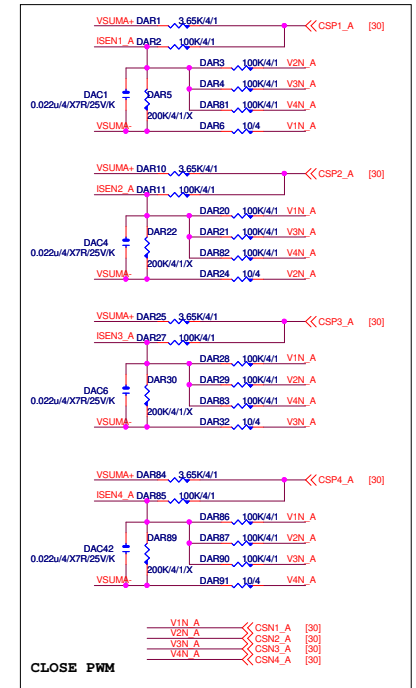
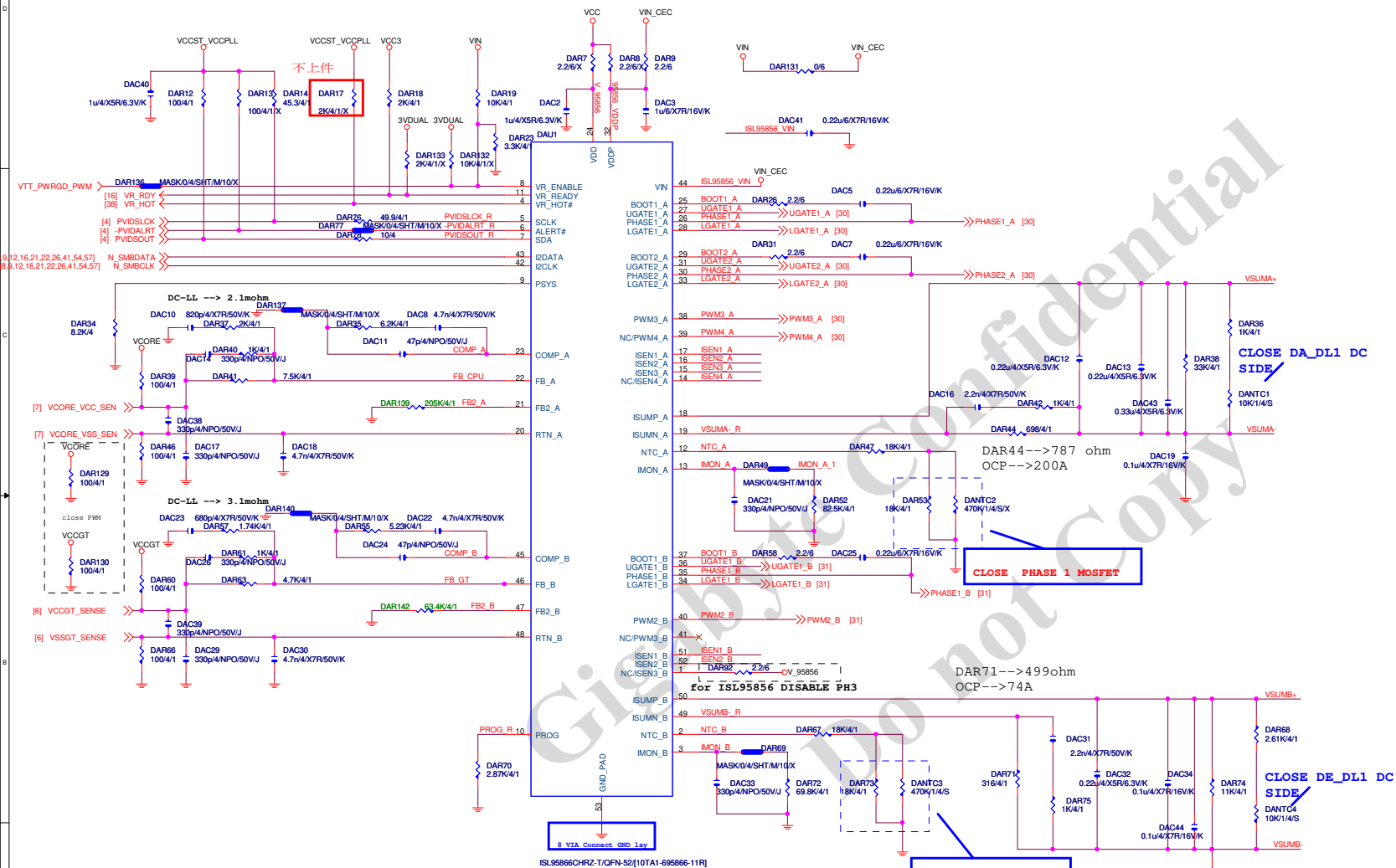
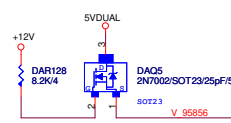


CEC:DAR133.DAR132 上件.DAR18.DAR19.DAR23.DAR131不上件

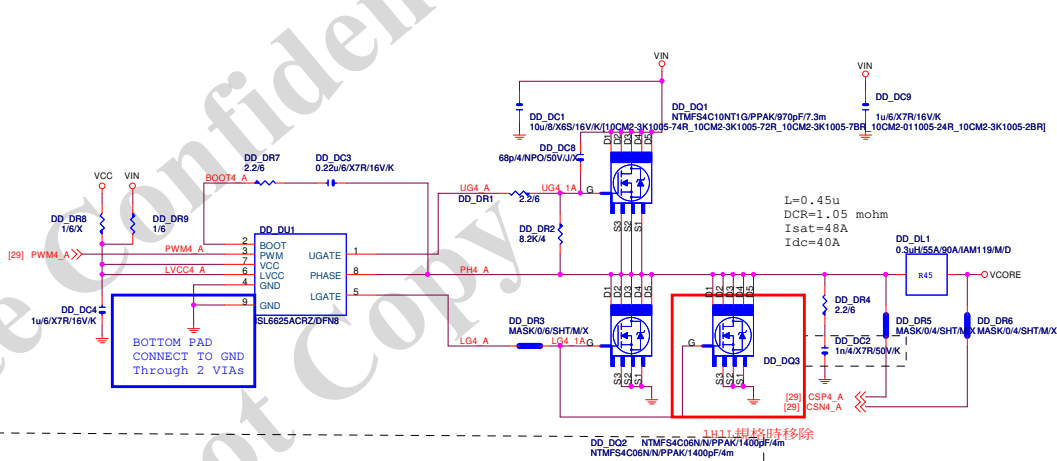
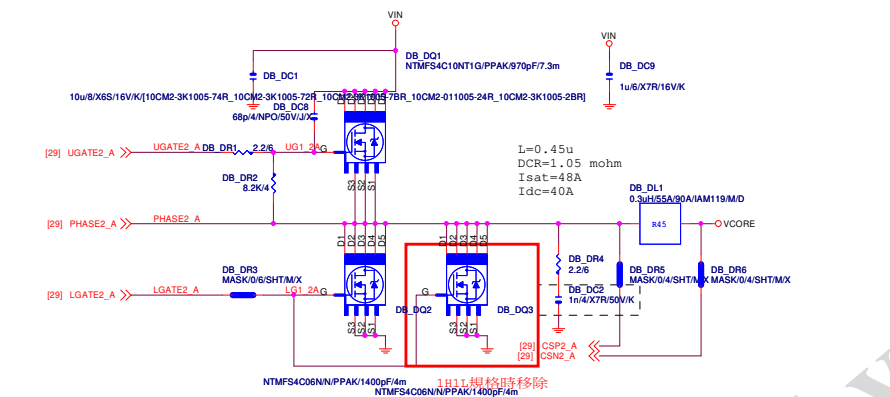
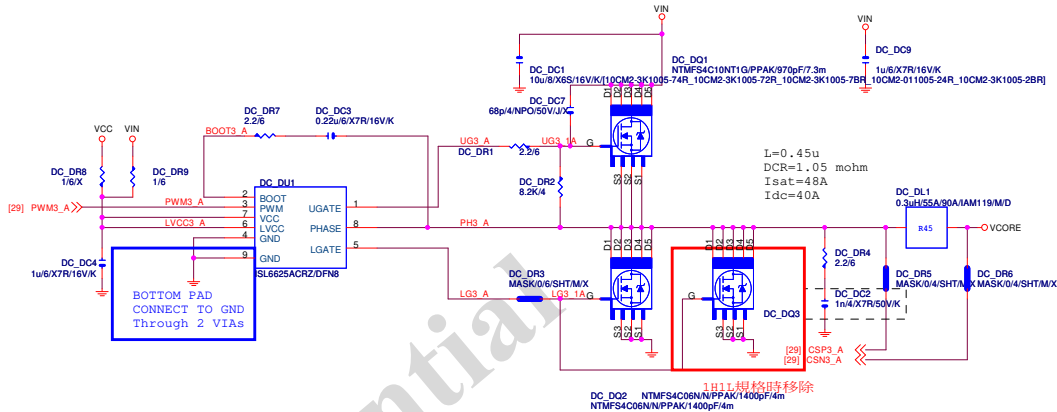
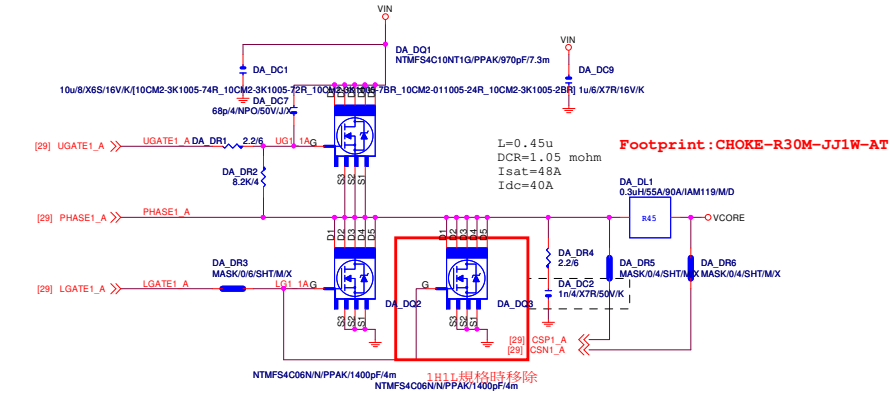
non CEC:DAR133.DAR132 不上件.DAR18.DAR19.DAR23.上件.

DAR131改short pad

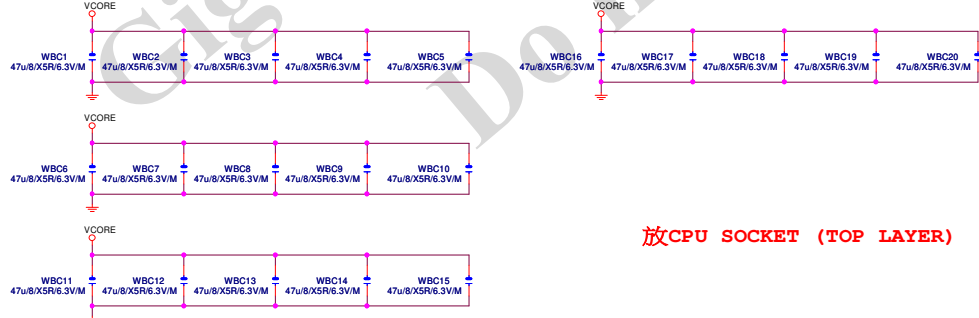
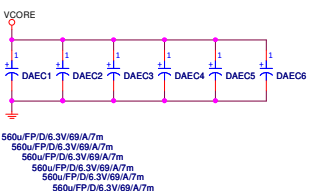
DAR131 short pad footprint:R0603-RH-SHORT30-MASK



VCORE

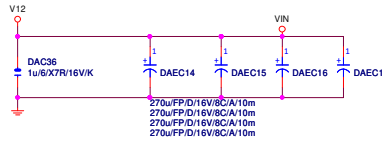


VCORE CAP 560u*6PCS 22u*20PCS

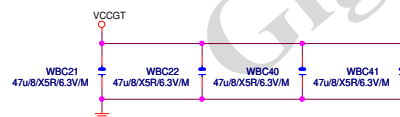
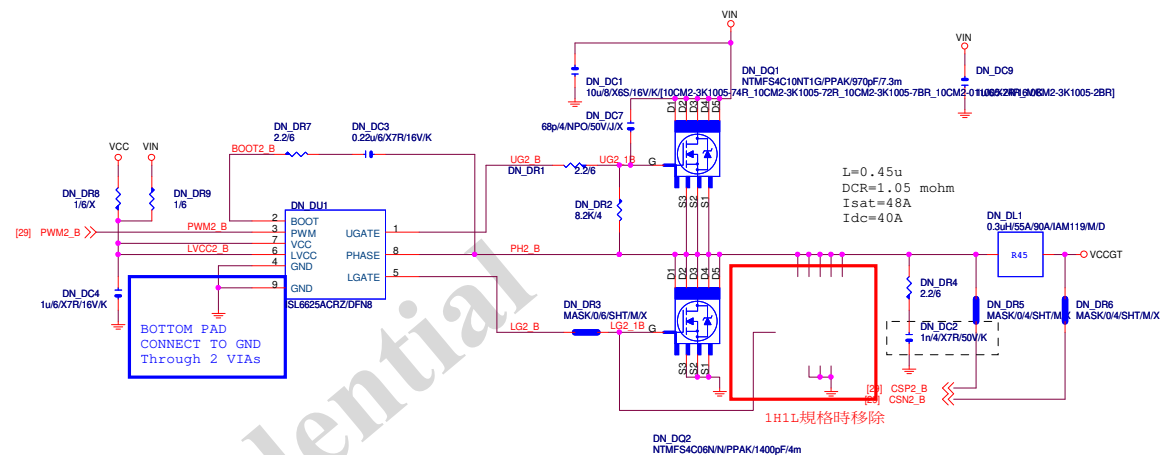


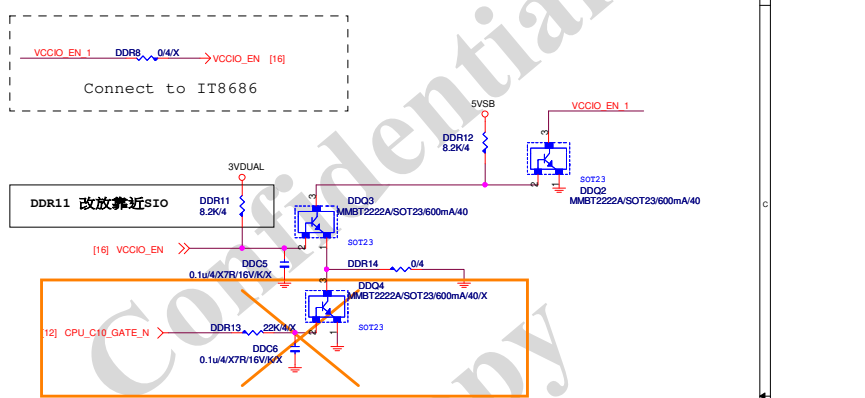
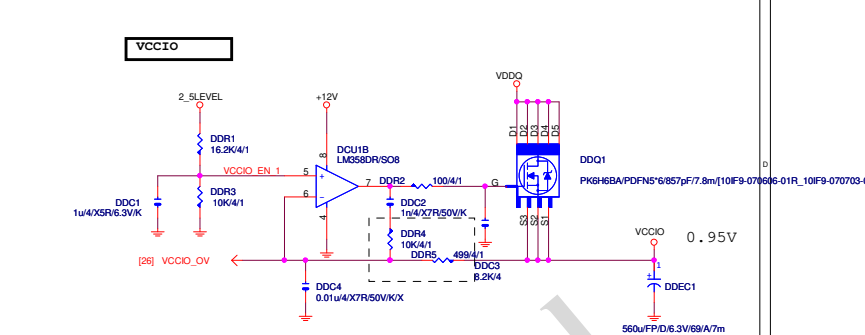
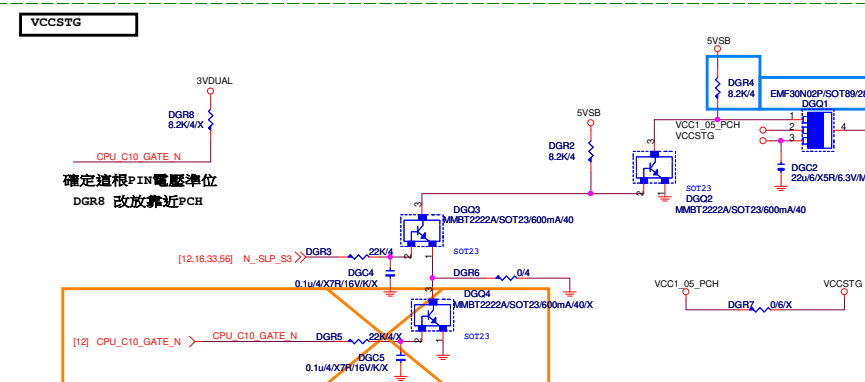
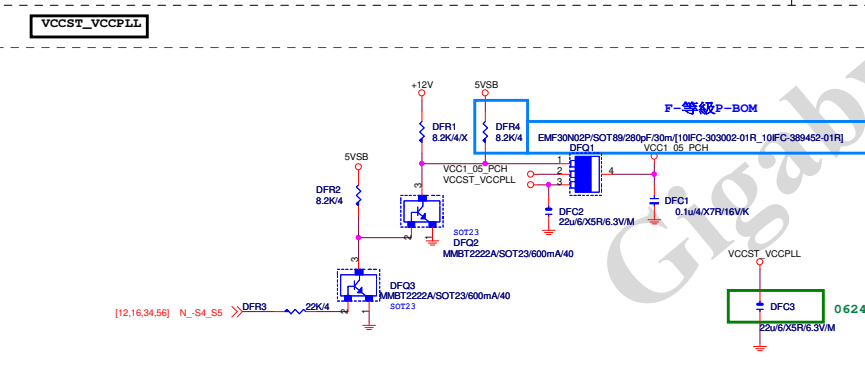
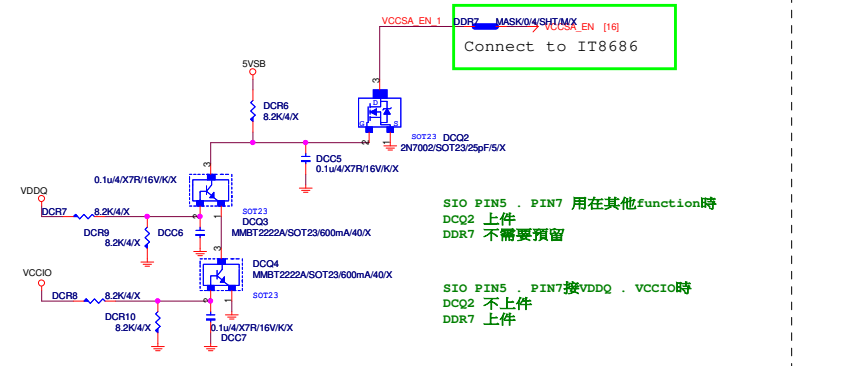
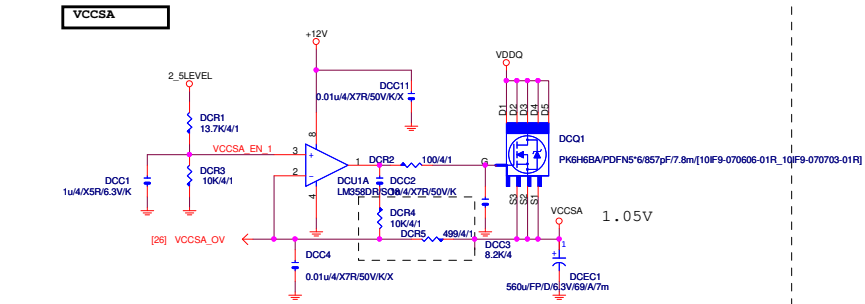
放CPU SOCKET (TOP LAYER)

VIN CAP 270u*4PCS

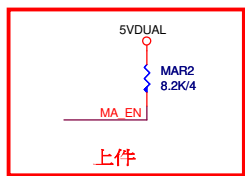


File		
ISL95866 MOS		
Size	Document Number	Rev
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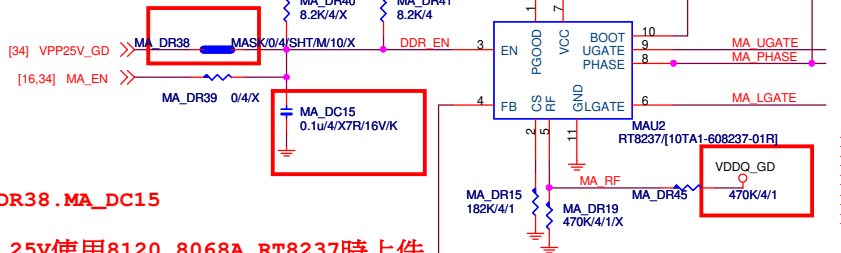




DDR4

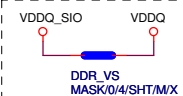


上件



MA_DR38.MA_DC15

VPP_25V使用8120、8068A、RT8237時上件

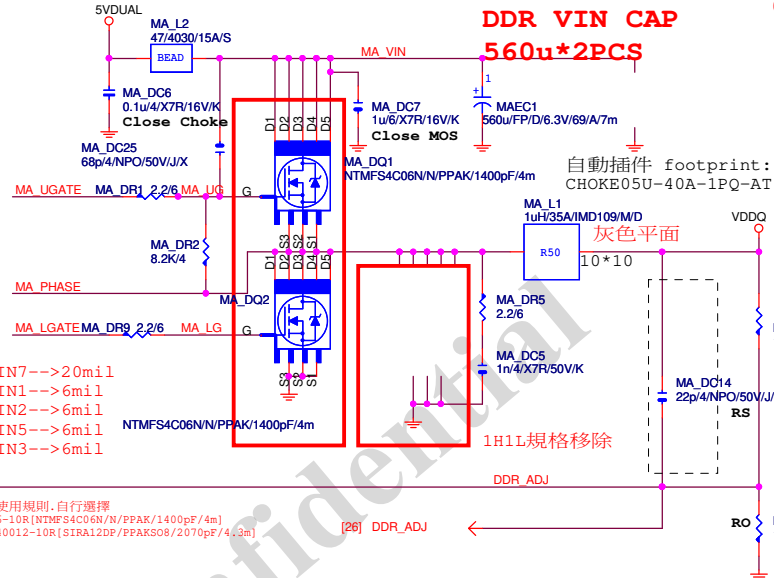


FS=290K MOSFET請依MOSFET使用規則,自行選擇
ON-->10IF9-040406-10R[NTMFS4C06N/N/PPAK/1400pF/4m]
OCB=40A VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKSO8/2070pF/4.3m]

OCP=40A

MOSFET請依MOSFET使用規則,自行選擇
ON-->10IF9-040406-10R[N1MFS4C06N/N/PPAK/1400pF/4m]
VISHAY-->10IF9-040012-10R[SIRA12DP/PPAKS08/2070pF/4.3m]

MAU1上RT9045時上件(不可MASK)



DDR VIN CAP

~~560u*2PCS~~

CHOKES與CAP料號可變

SUPPORT DDR4 1.2V

1.2V

25A MAX

L=1u
DCR=2.5 mohm
Isat=35A
Idc=28A

請放置CHOKE一出來位置.先預留.
請自行確認ripple後再決定是否上件

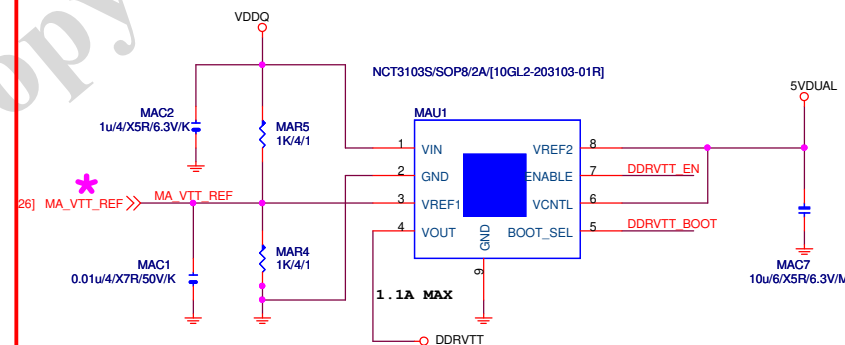
Remote sense 請從最重的負載端點拉回

PWR SEQ

CLOSE TO DDR POWER PLANE

For power sequence require

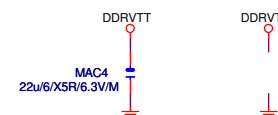
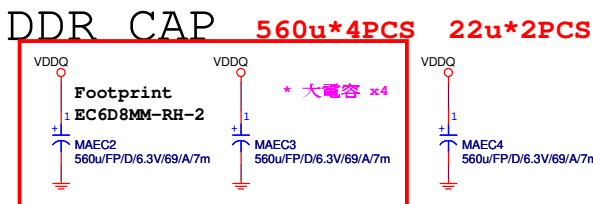
VPP_25V使用8120時上件

DDRVTT

[4] DDR_VTT_CTL >> DDR VTT CTL MAR110 MASK/0/4/SHT/M/10/X DDRVTT_EN
[12 16 32 56] N_SLP_S3 >> N_SLP_S3 MAR111 MASK/0/4/SHT/M/10/X DDRVTT_BOOT

DDRVTT CAP

* 大電容 x0



GIGABYTE

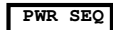
Title	RT8237 DDR4 POWER
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Size	Document Number
Custom	B460M DS3H AC

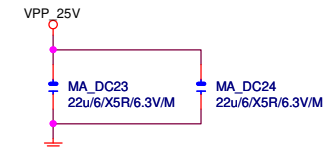
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VPP 25V

L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A



The schematic diagram illustrates the PWR_SEQ circuit. It features three MOSFETs (MAQ7, MAQ8, and MAQ9) connected in series between the VPP25_EN supply and ground. The gates of these MOSFETs are driven by the signals [12,16,32,56] N_S4_S5 and [16,33] MA_EN through resistors MAR106, MAR14, and MAC10 respectively. The source-drain paths include resistors MAR109 and MAC8. The MOSFETs are labeled as MAQ7, MAQ8, and MAQ9, all specified as 2N7002/SOT23/25pF/5/X.

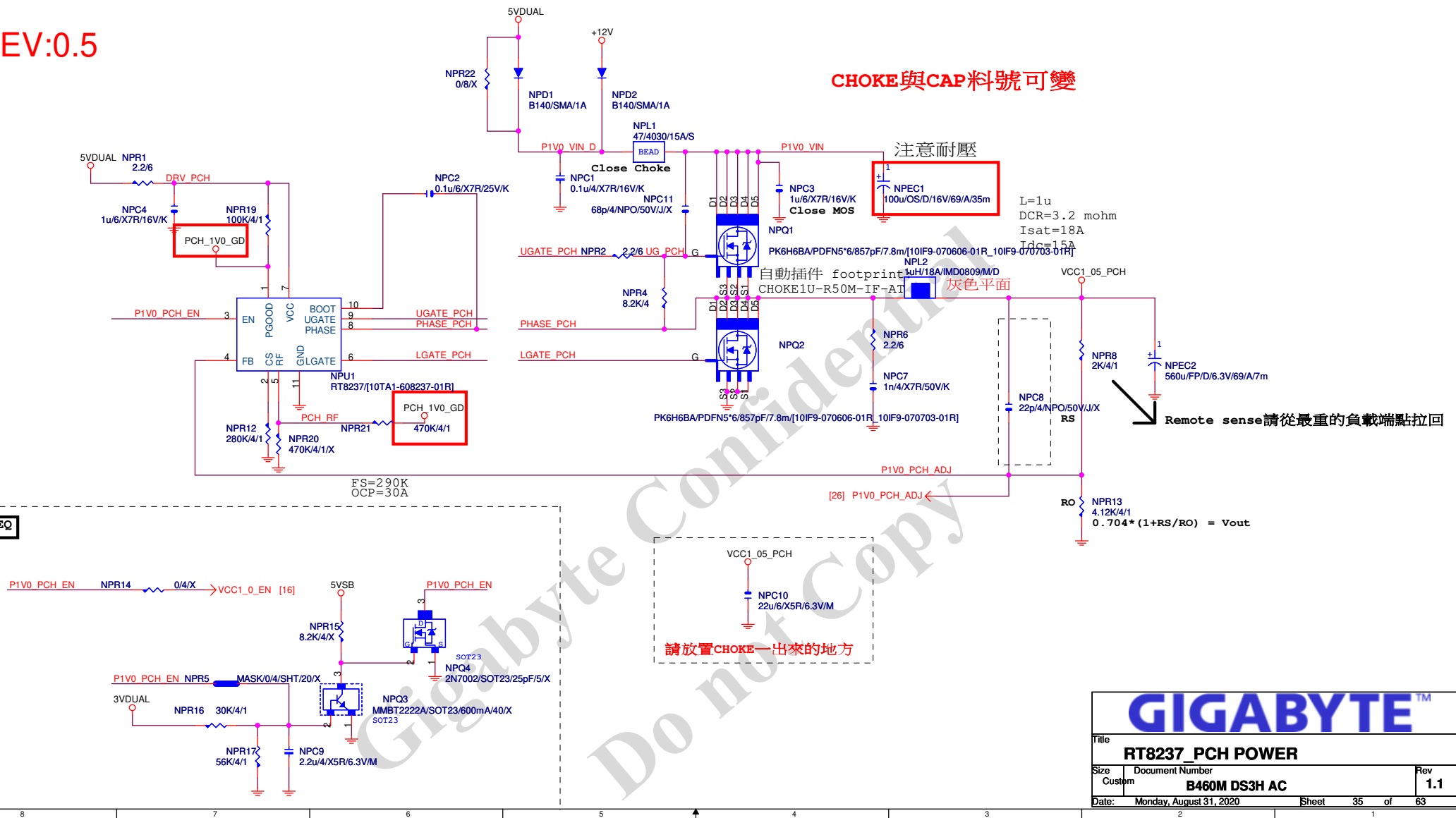


GIGABYTE™

Title			
RT8068A_VPP25 POWER			
Size	Document Number	Rev	
Custom	B460M DS3H AC	1.1	
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REV:0.5

CHOKE與CAP料號可變



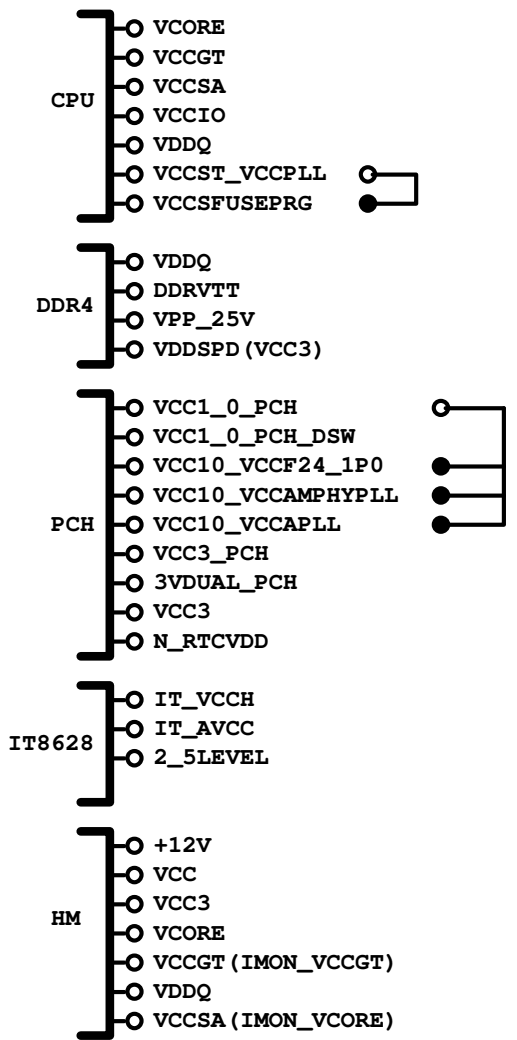
[16] 5VAUX_SW >>



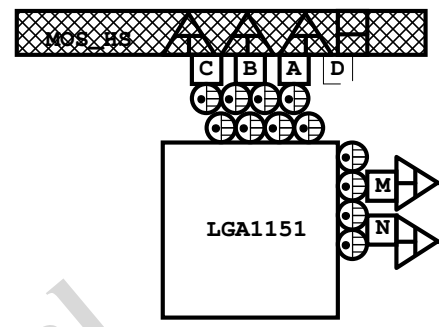
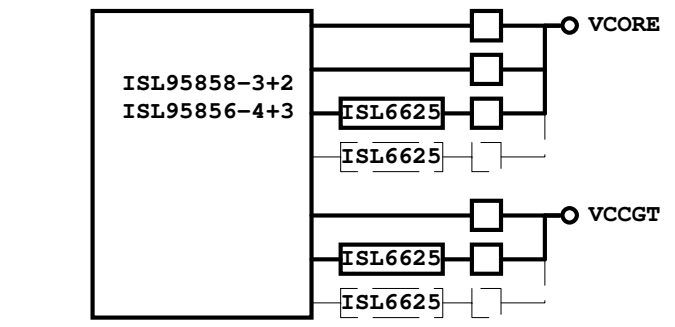
3VDUAL_PCH



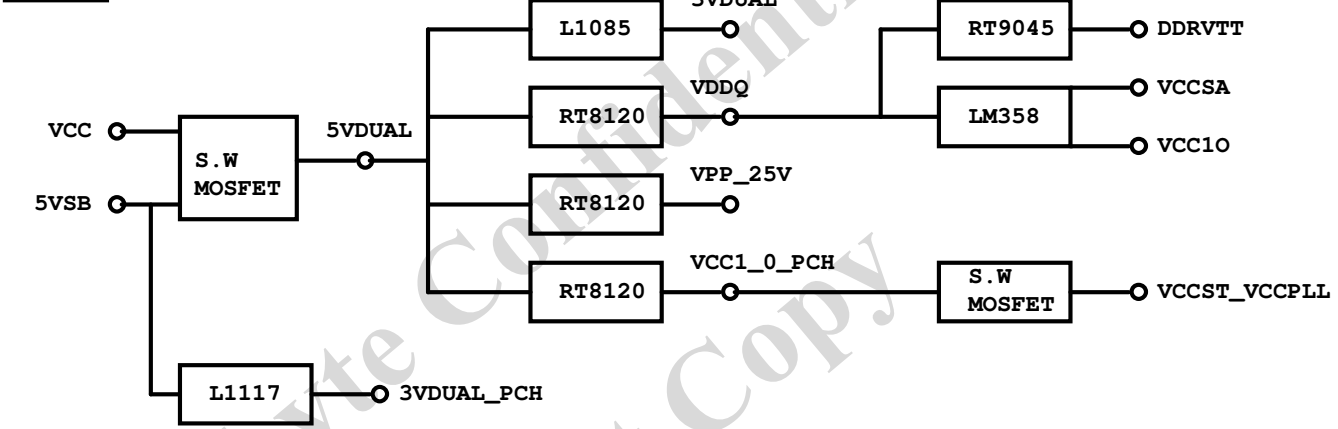
POWER BLOCK MAP



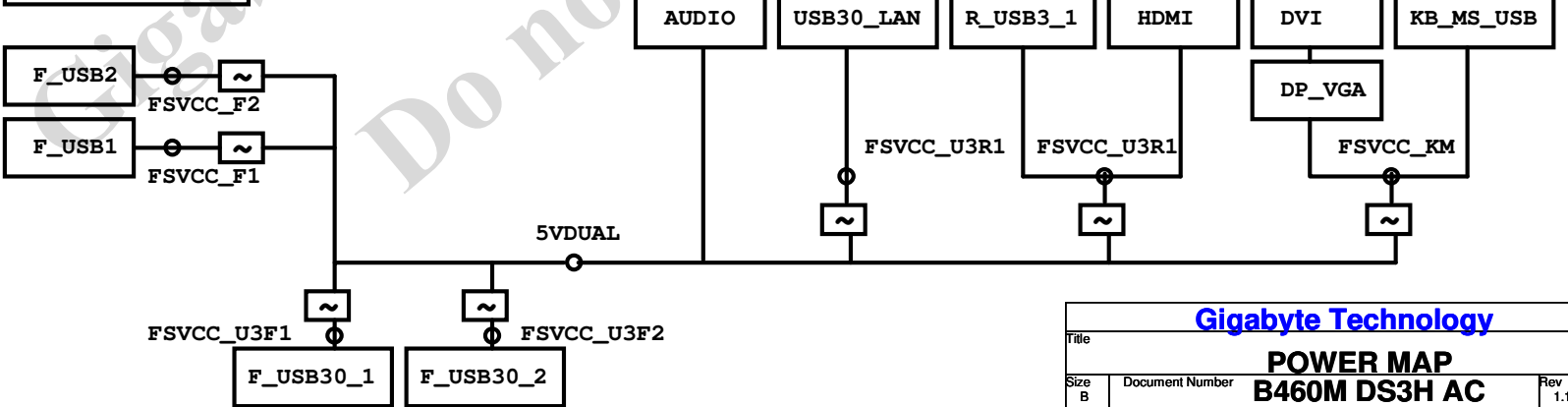
VCORE/VCCGT



POWER

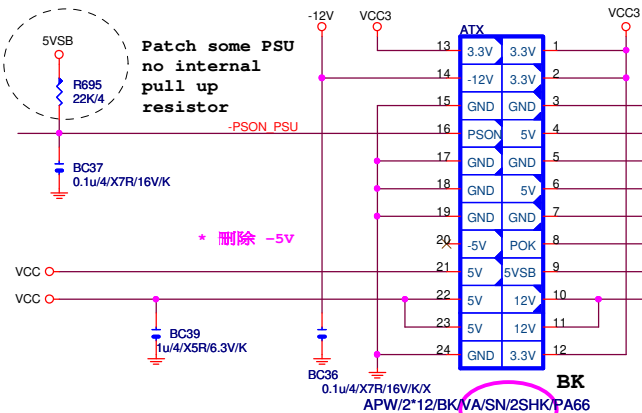


FUSE POWER F/R

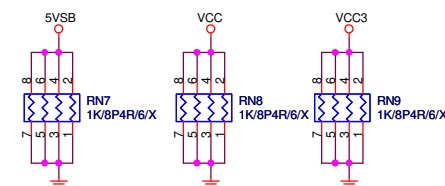


ATXX24 POWER CONNECTOR

2x12 (一般Pin)
FOOTPRINT: ATXPWR_24-6

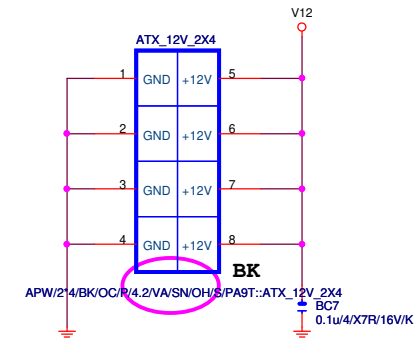


DUMMY LOAD

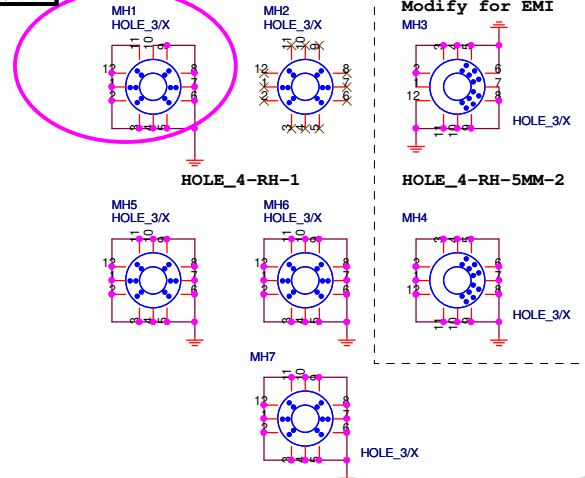


ATXX4 POWER CONNECTOR

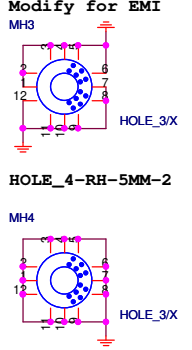
2x4 (實心Pin)
FOOTPRINT: ATXPW2X4-SOLID



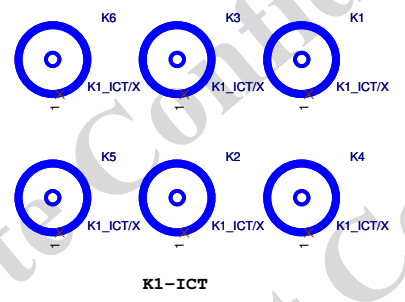
螺絲孔



14/12/24



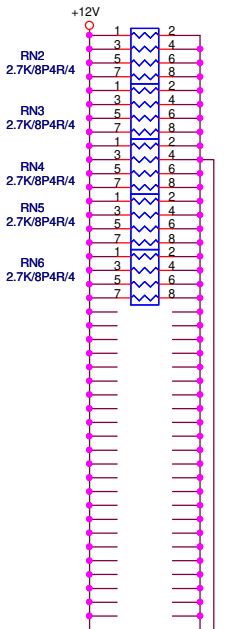
固定孔/光學點



+12V DUMMY LOAD

【技術通報R&D技術通報153】

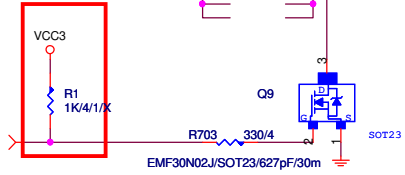
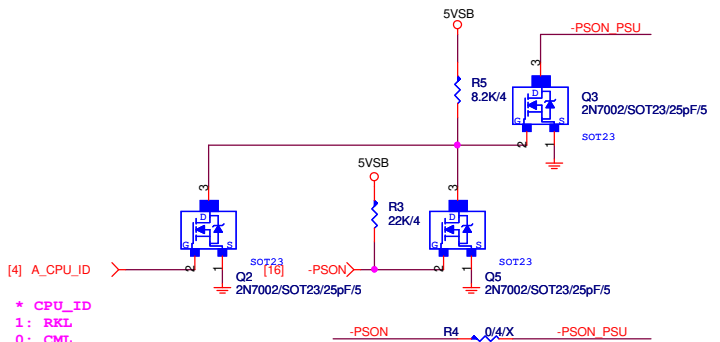
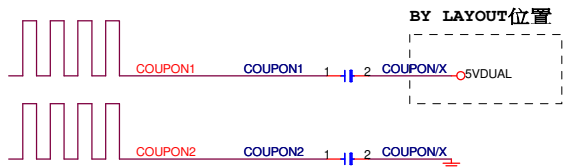
To fix 12V light load abnormal issue

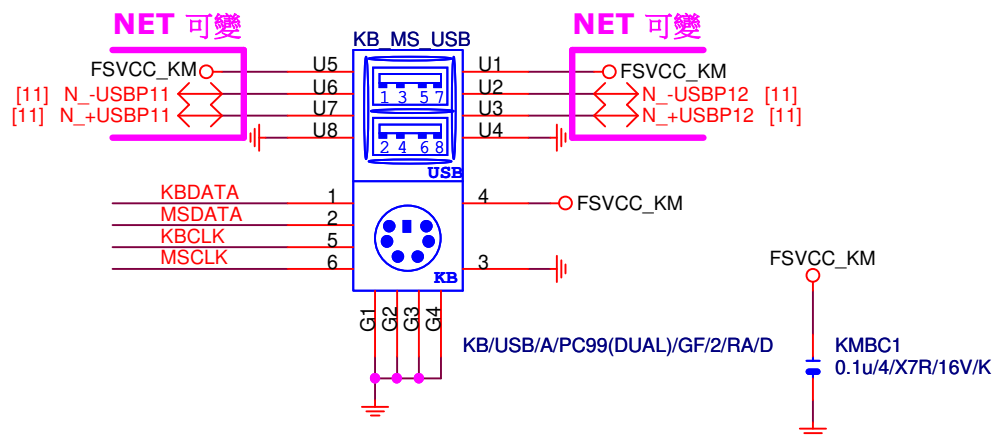


-PROHOT

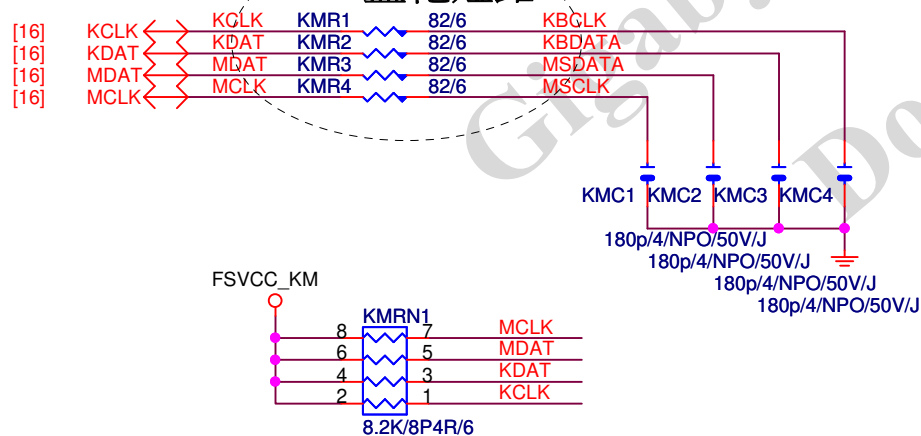


COUPON



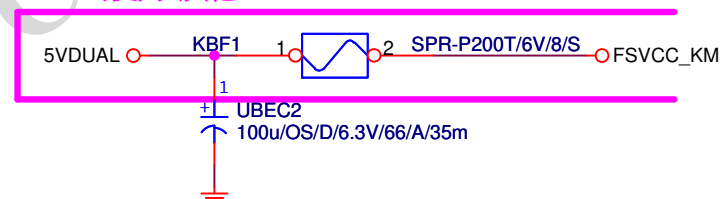
Rev: 0.7

FOR鹽化短路



The schematic diagram illustrates the USB-to-serial bridge circuit. It consists of two AZC099-04S/SOT23-6L chips, labeled KMED2 and KMED1. The top chip, KMED2, is connected to the USB signals N_+USBP12, N_-USBP12, N_-USBP11, and N_+USBP11. The bottom chip, KMED1, is connected to the USB signals KBCLK, KBDATA, MSCLK, and MSDATA. Both chips are connected to a common FSVCC_KM pin, which is also connected to a 10k resistor and a 100nF capacitor.

NET 可變，與其他USB SHARE

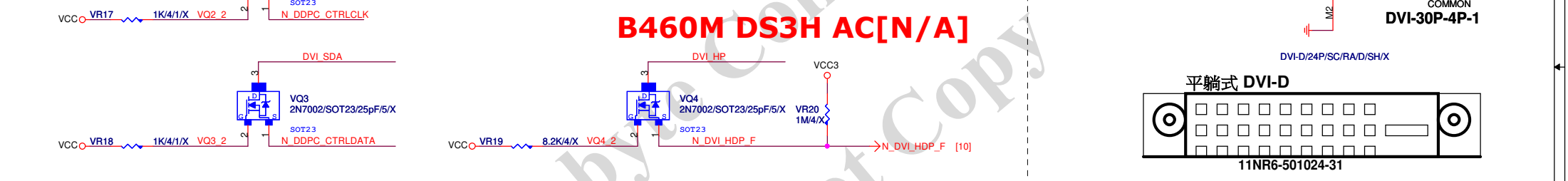
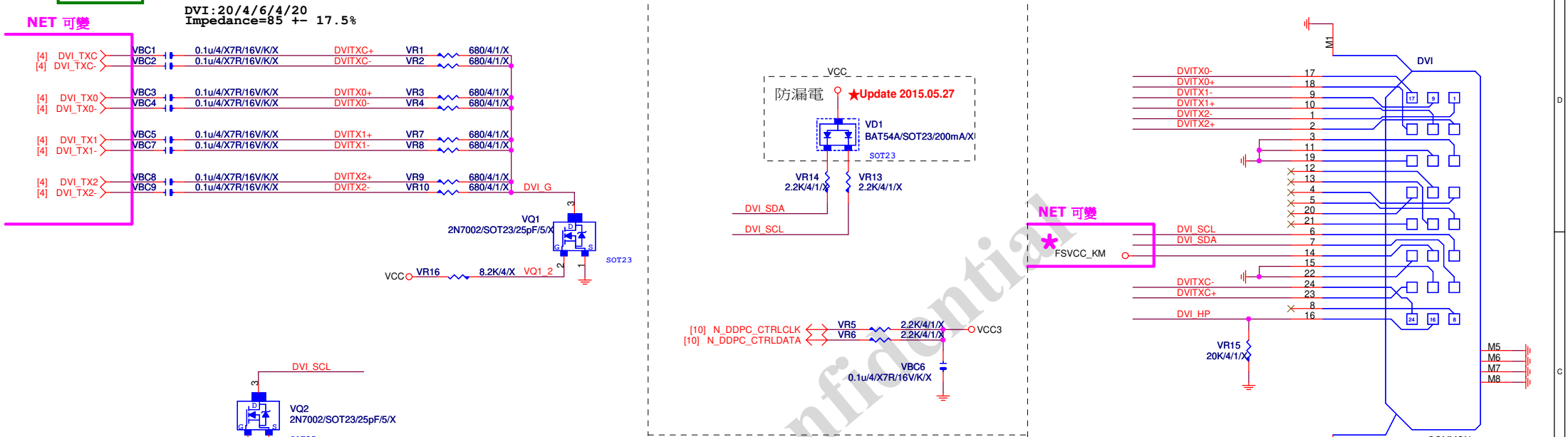


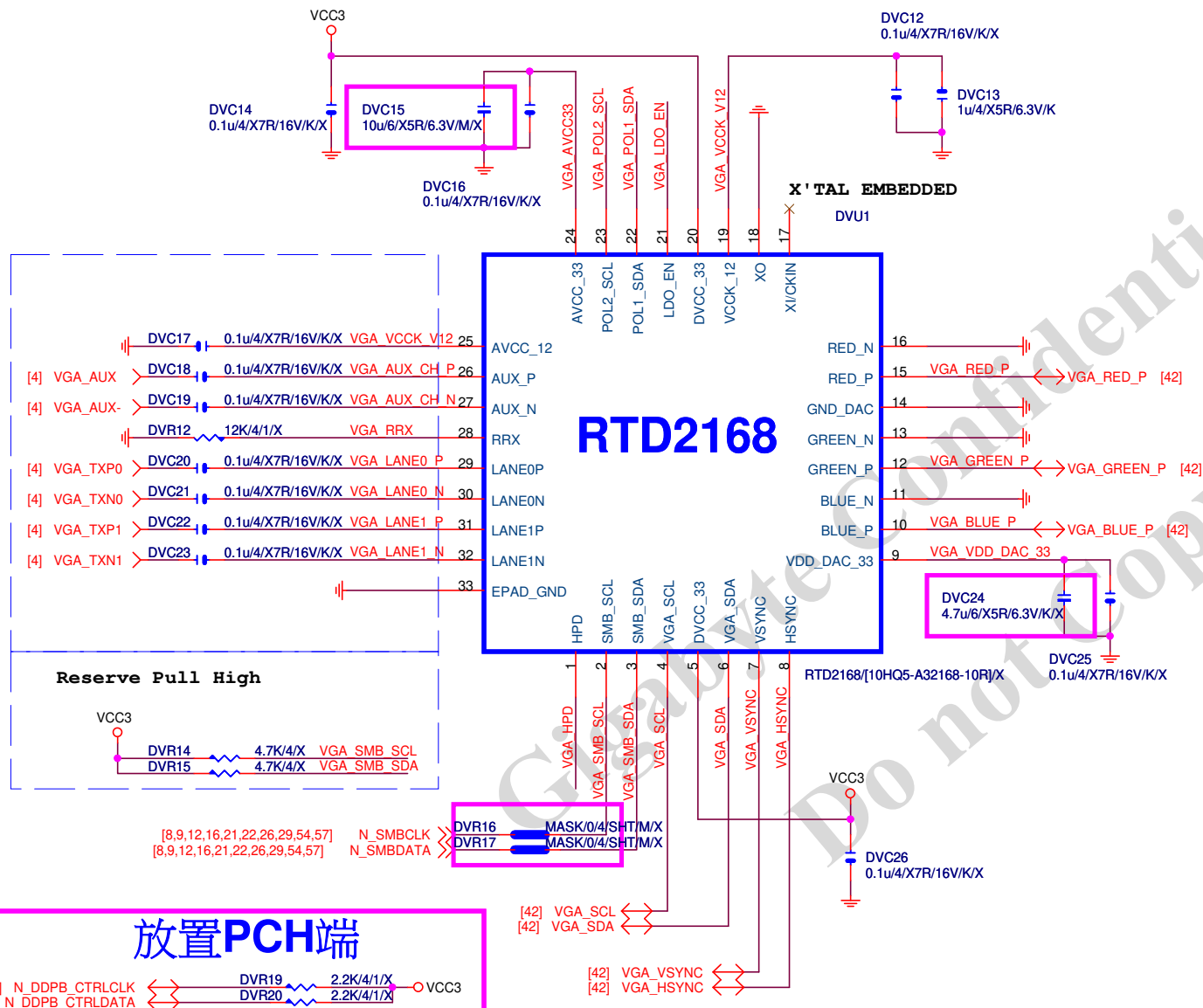
Gigabyte Technology

KB MS USB

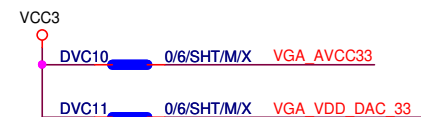
B460M DS3H AC

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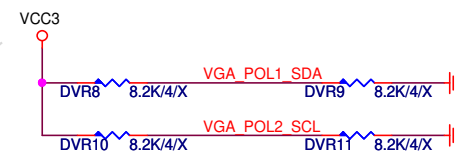




B460M DS3H AC[N/A]

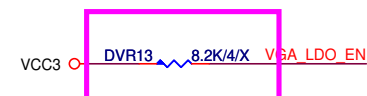
POWER

Power on latch



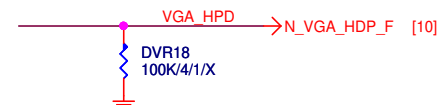
		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

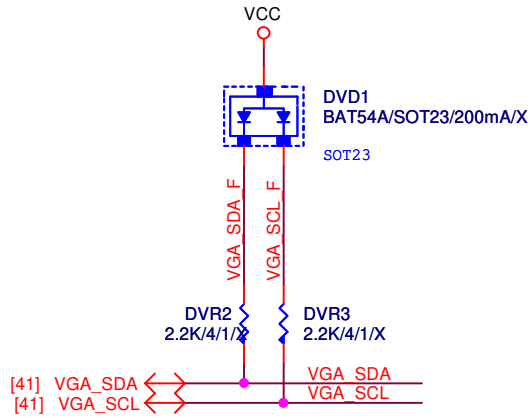


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

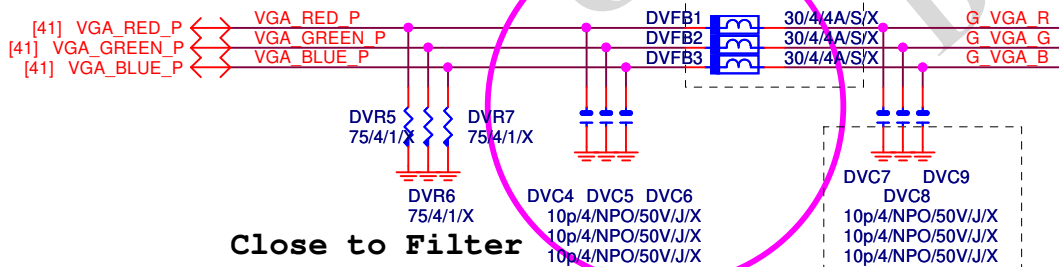
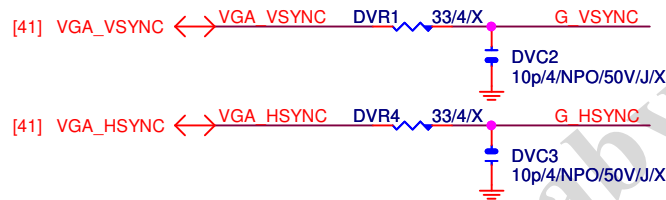
DP HPD



VGA SIGNAL R2.0



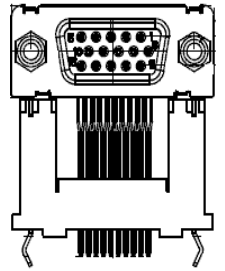
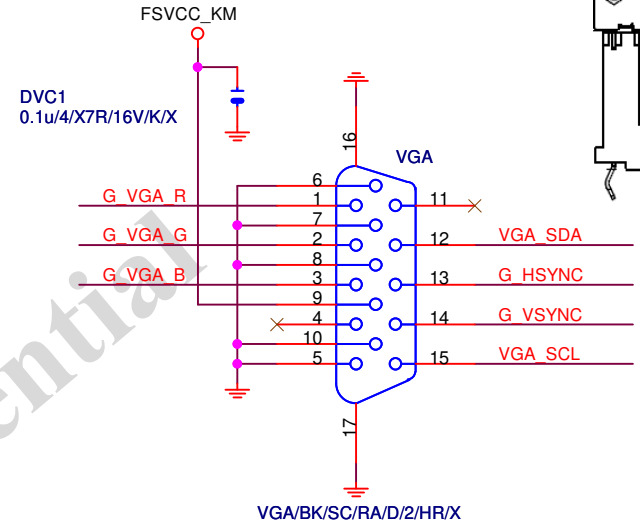
B460M DS3H AC[N/A]



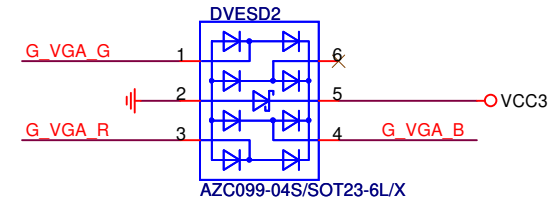
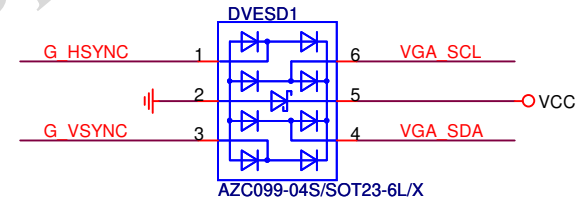
Close to Filter

FOR EMI

VGA CONN. 架高型VGA (BLACK)



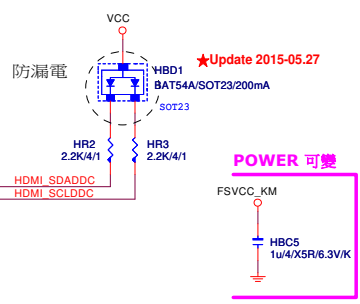
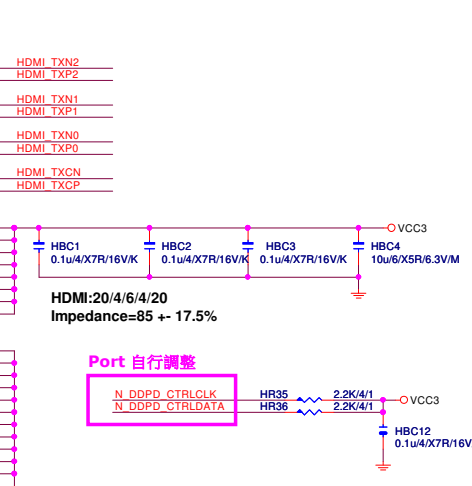
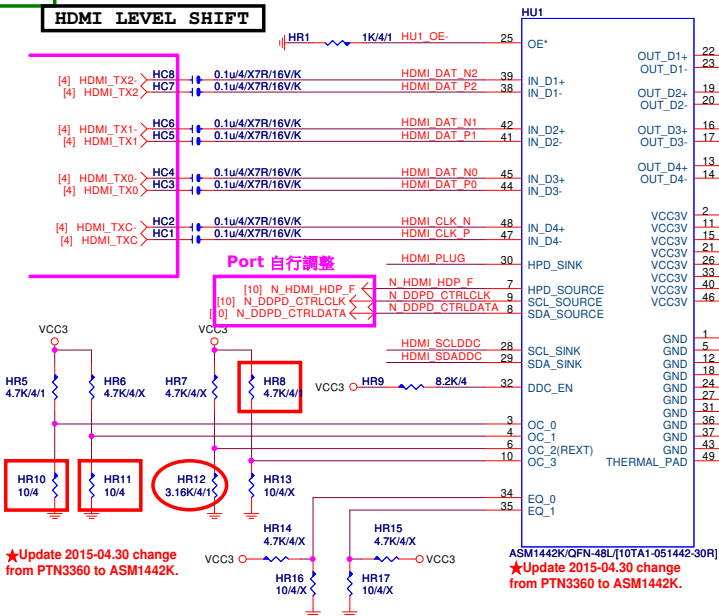
VGA ESD



Gigabyte Technology
DP-VGA RTD2168

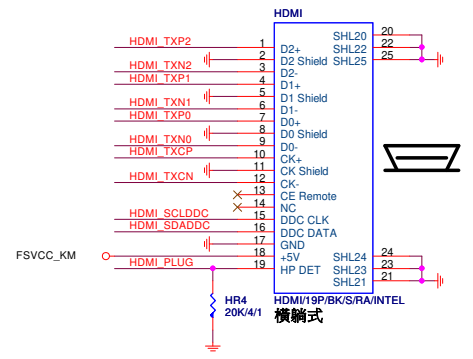
Title		
Size	Document Number	Rev
Custom	B460M DS3H AC	1.1
Date:	Monday, August 31, 2020	Sheet 42 of 63

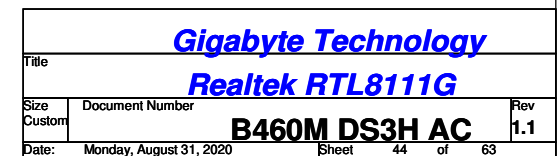
HDMI LEVEL SHIFT



【技術通報R&D技術通報150】
HDMI eye diagram 1.4版 (deep color) 會fail
原因: 因目前的HDMI訊號過長, 造成RISING TIME過慢, 而會壓到eye diagram
改善: ASMEDIA ASM1442 : 3.16K (PIN6 PULL DOWN電阻) 10ohm (PIN4 PULL DOWN電阻)

PTN3360: PIN 4/10/34/35 NC PIN, 都不上值; 只上HR12: 10K
ASM1442: 紅色框要上, HR12: 3.16K

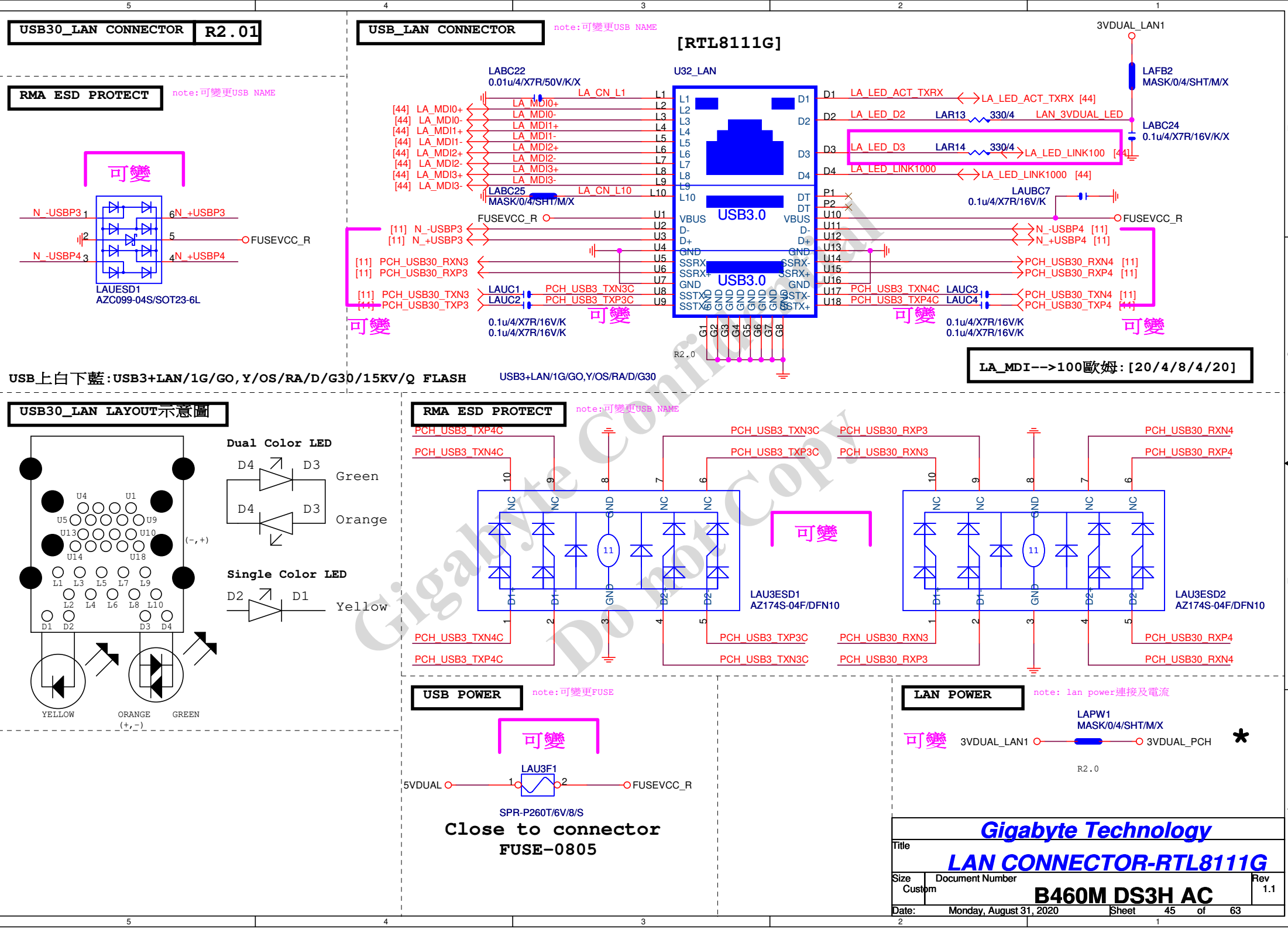




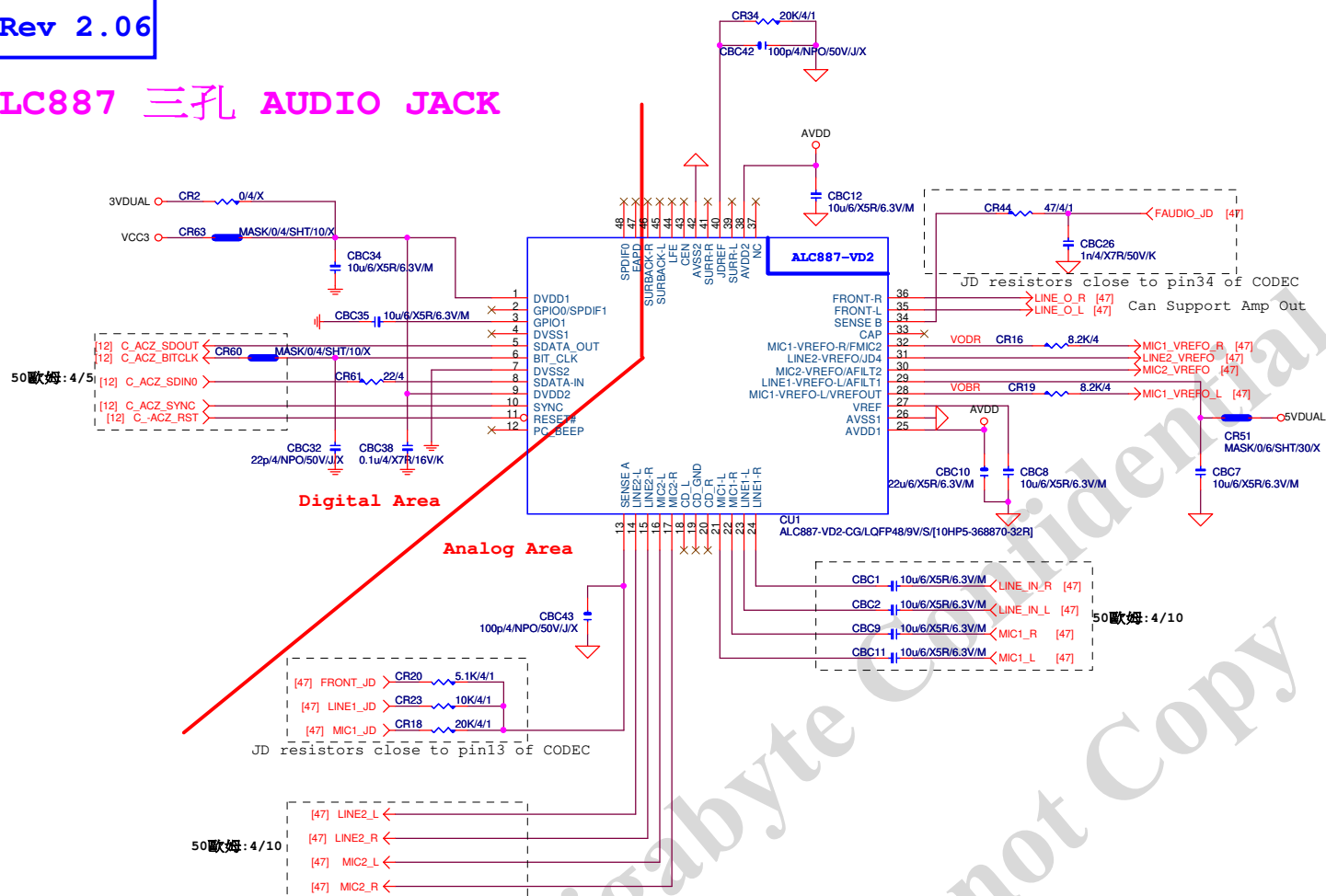
Sheet 44 of 63

B460M DS3H AC

Rev
1.1



ALC887 三孔 AUDIO JACK



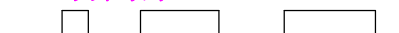
LAYOUT注意: 螺絲孔下GND方式

- MH1空間夠, 下DGND
- 空間不夠, 改為Isolate
- MH2一律改為Isolate

<input type="radio"/> MH1	<input type="radio"/> MH2
DGND	Isolate

LAYOUT注意: 要加

GND切割線



音效區域印刷



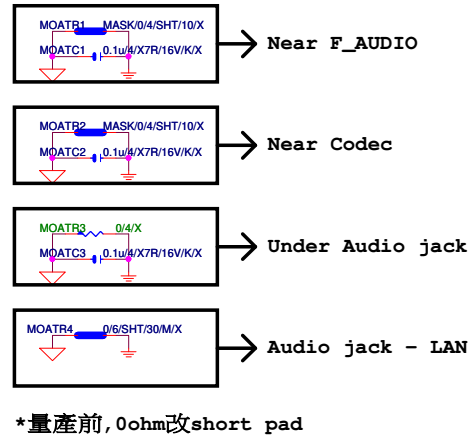
*料號後補
*LAYOUT與否, 依照各Model spec

BOM OPTION :

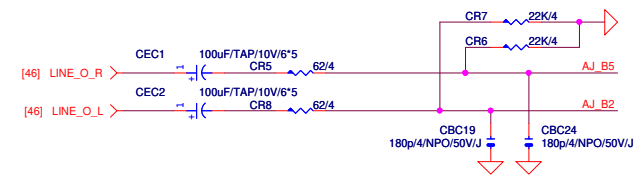
- Chemicon音效電容
- 金屬外罩 Reserve (上件與否, 依照各Model spec)
- LED Reserve (上件與否和LED顏色, 依照各Model spec)

Gigabyte Technology			
HD AUDIO ALC887			
Size	Document Number	B460M DS3H AC	
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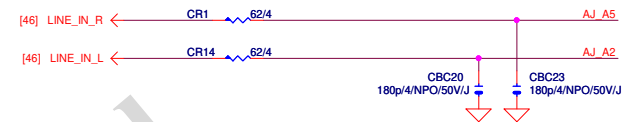
Rev 2.06



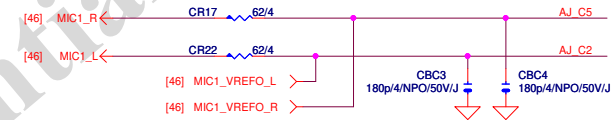
LINE-OUT



LINE-IN



MIC-IN

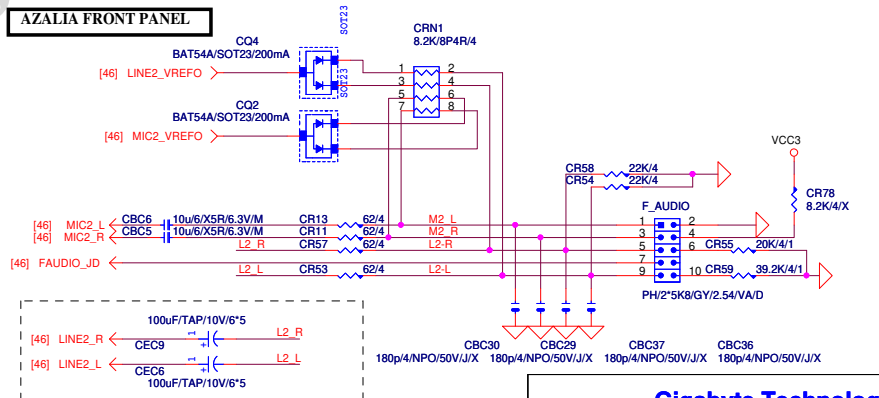


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL



Gigabyte Technology

AUDIO JACK

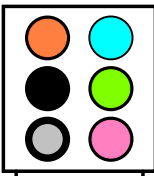
B460M DS3H AC

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For HDMI SPDIF (依SPEC保留或移除)

AZALIA JACK

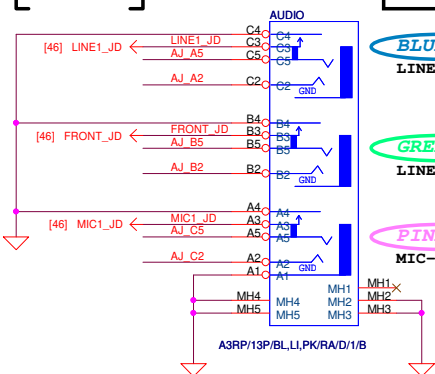


AZALIA JACK

BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN

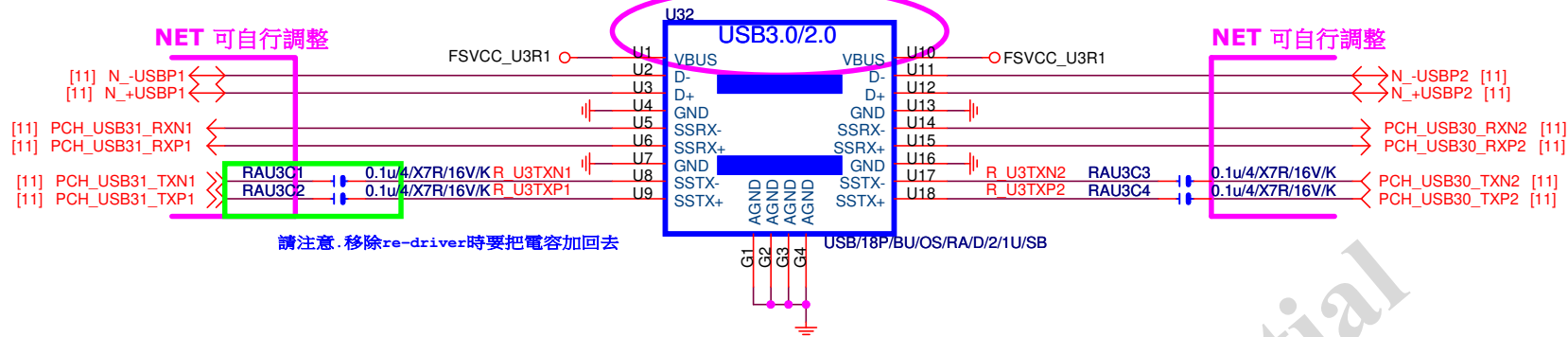


Gigabyte Confidential
Do not Copy

GIGABYTE™			
Title Amient Single LED			
Size Custom	Document Number B460M DS3H AC		Rev 1.1
Date:	Monday, August 31, 2020	Sheet 48 of 63	

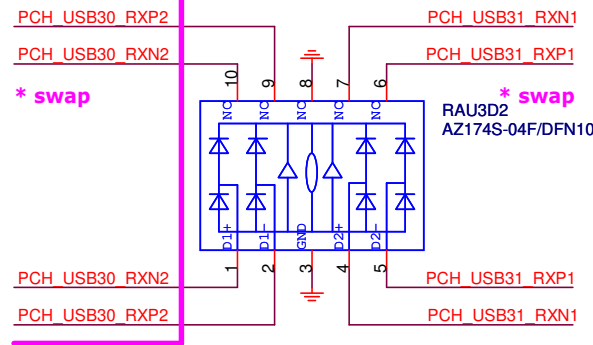
Rev: 0.7

ESD 可自行SWAP PIN ,CONN端 NET 名稱 不可

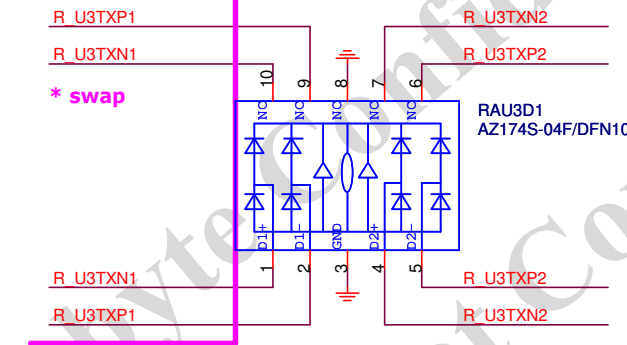


ESD

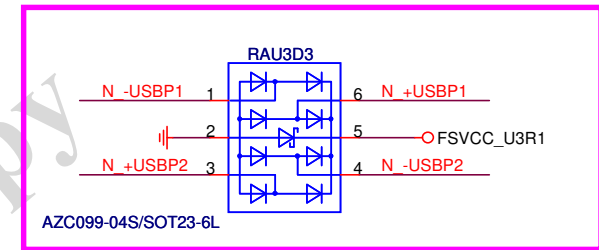
NET 可自行調整



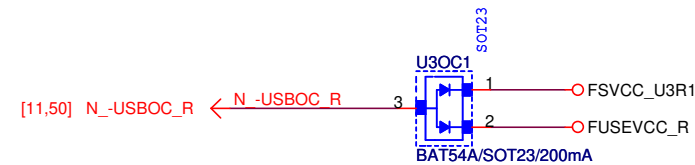
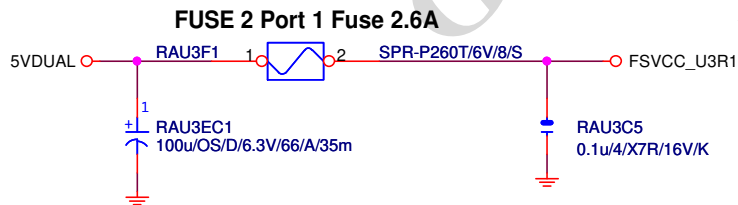
NET 可自行調整



NET 可自行調整



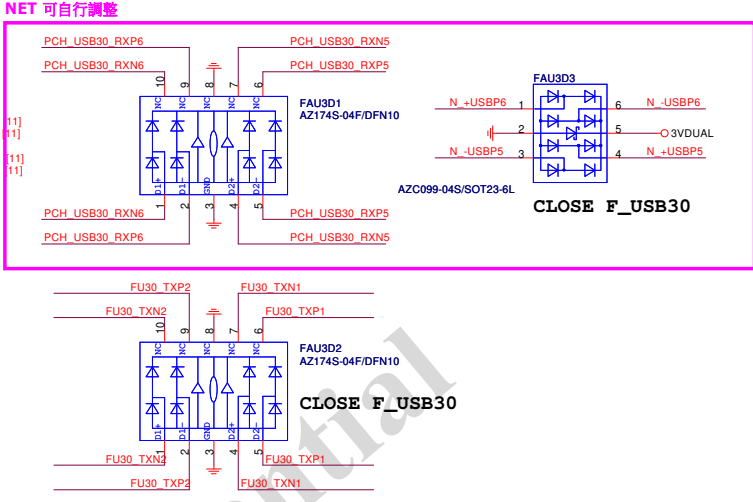
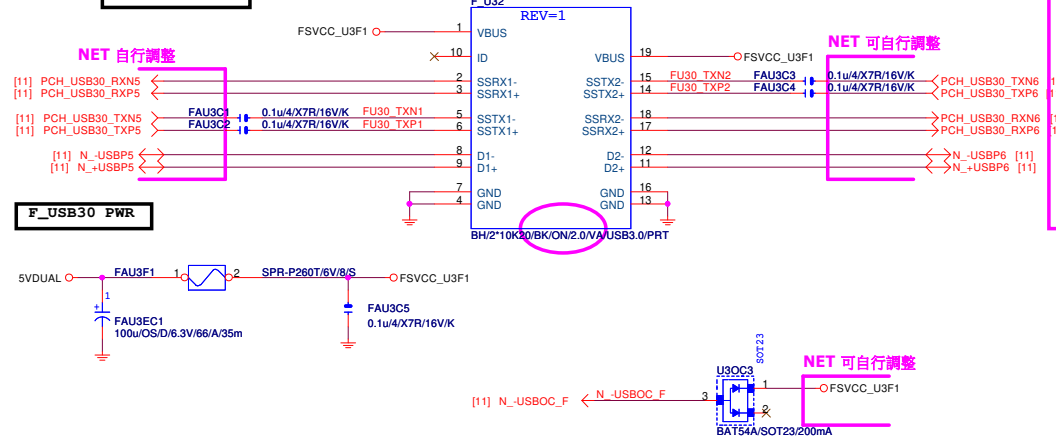
FUSE



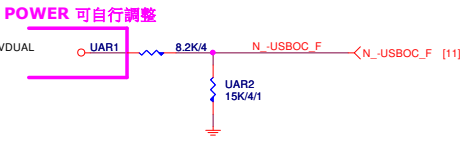
Gigabyte Technology

Title				Rev 1.1
R_USB30,USB_OC				
Size Custom	Document Number			B460M DS3H AC
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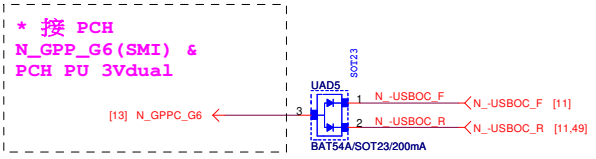
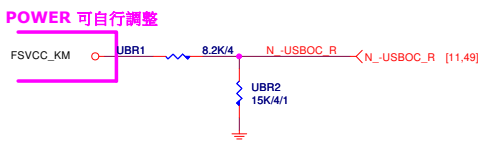
Front USB3.0



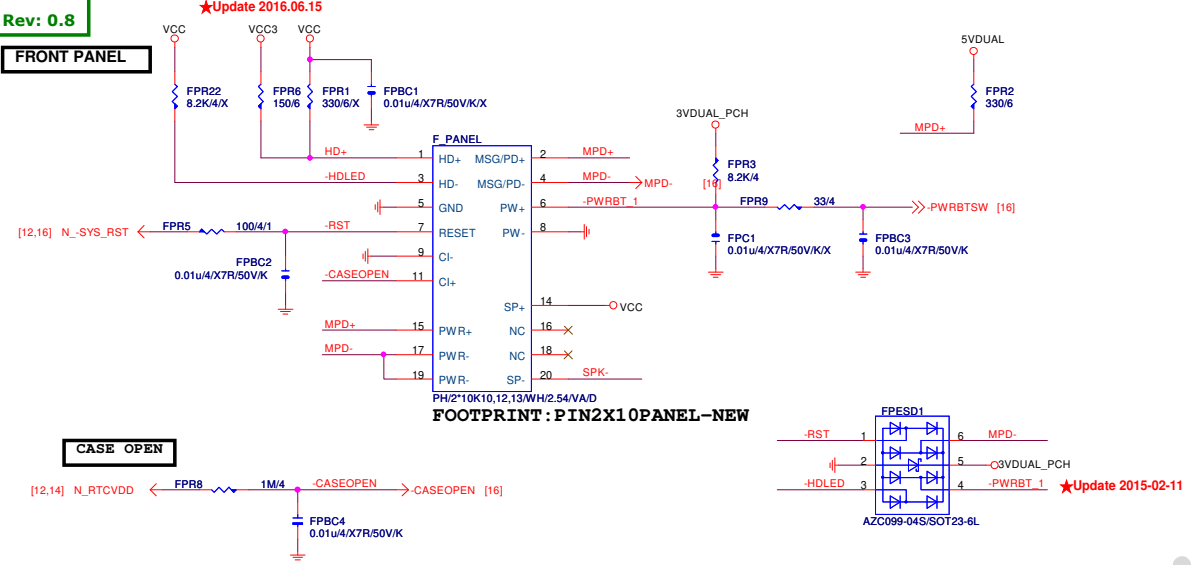
-USBOC_F



-USBOC_R



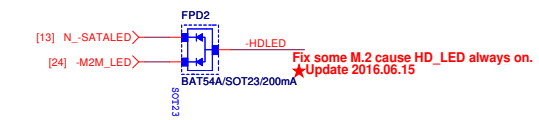
FRONT PANEL



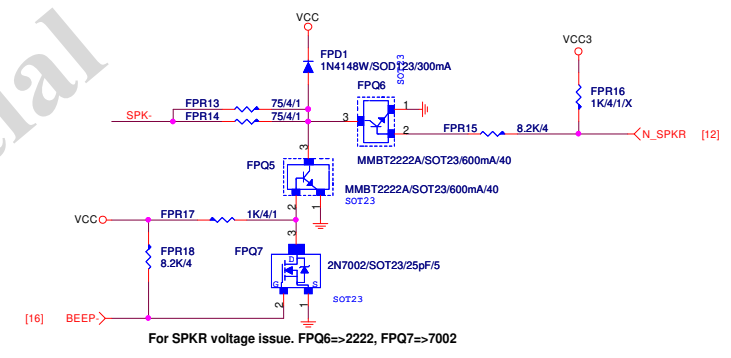
CASE OPEN

FRONT PANEL SHORT

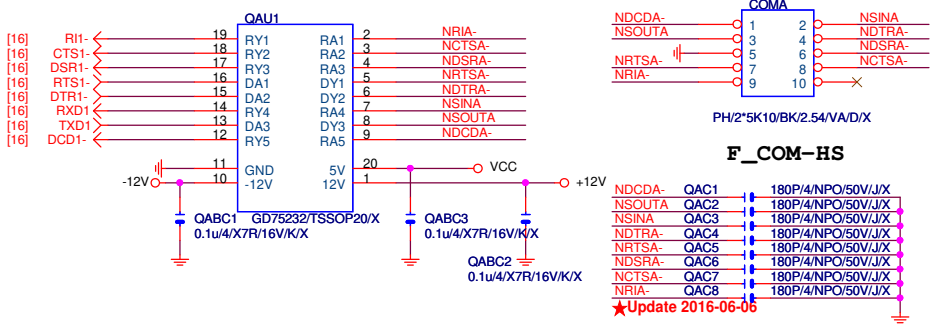
SATA/M.2 LED



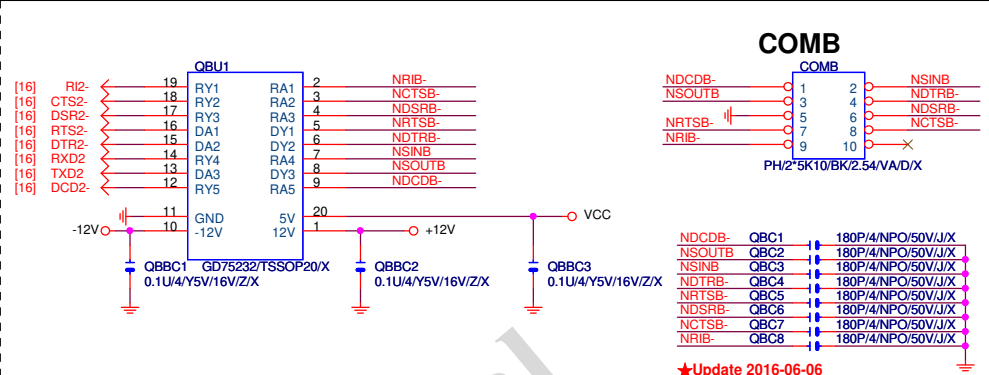
SPKR



COM PORT Rev: 0.7



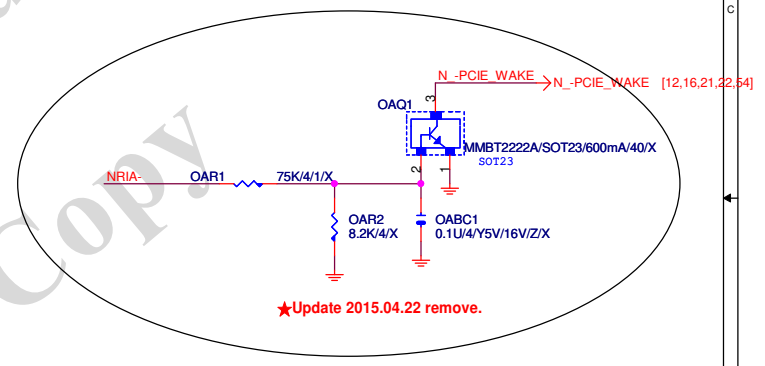
B460M DS3H AC[N/A]



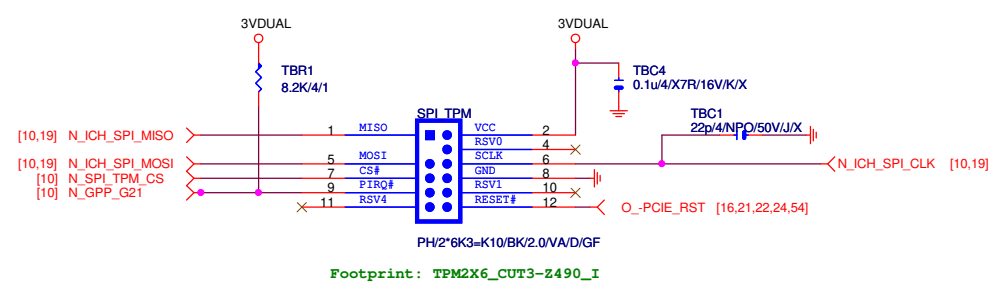
B460M DS3H AC[N/A]

LPT PORT

COM RI N/A



TPM CONNECT



Rev: 0.2

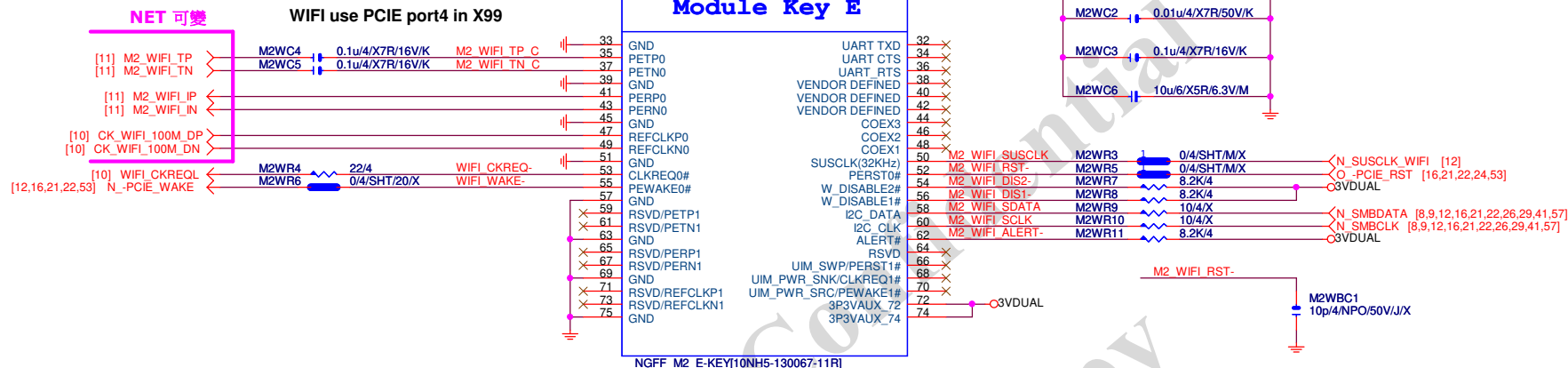
請選擇適用的USBport :
SOC/UD7/UD5/G1/G7 : USB4
;UD3/G5:USB6

NET 可變

[11] N_+USBP10
[11] N_-USBP10

PCIE:15/4/4/15(breakout min 8/4/4/8)
外層Impedance=85 +- 17.5%

PCIE:15/4/4/15(breakout min 8/4/4/8)
內層 Impedance=85 +- 12%



一套WIFI MODULE包含外框+WIFI CARD+天線



Footprint WIFI-EKEY+ WIFI-EKEY-MODULE should be a package.

GIGABYTE™

Title M2 WIFI		
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CLOSE SIO

EMIC1
100p/4/NPO/50V/J/X

[12,15,32,33] N_SLP_S3 ←

EMIC2
100p/4/NPO/50V/J/X

[12,16,32,34] N_S4_S5 ←

CLOSE PCH

EMIC4
100p/4/NPO/50V/J/X

[4,12] N_CPUPWROK ←

CLOSE NR47

VCC3

EMIC3
0.1u/4/X7R/16V/K**GIGABYTE™**

Title

EMI/ESDSize
A

Document Number

B460M DS3H AC

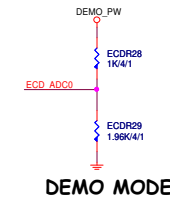
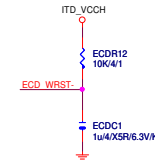
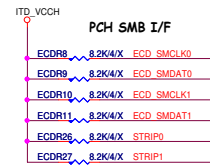
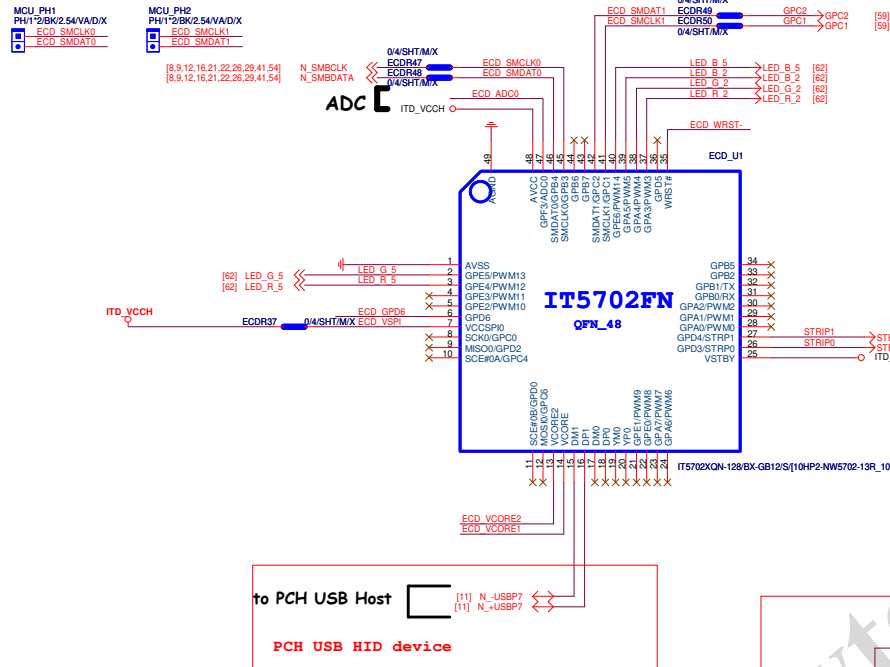
Rev

1.1

Date: Monday, August 31, 2020

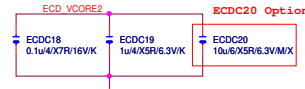
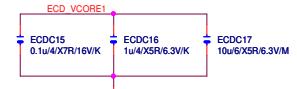
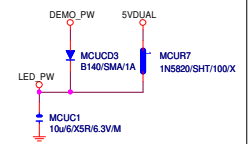
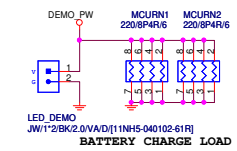
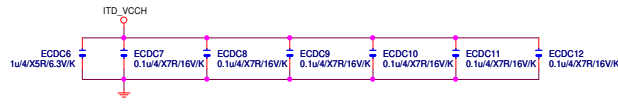
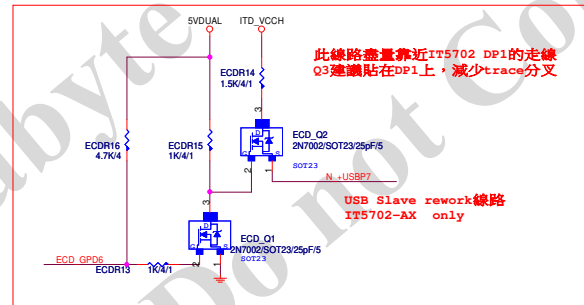
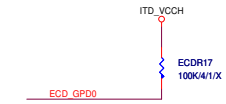
Sheet 56 of 63

ECD_U1 請放在PCH到BIOS路徑上. 避免線過長



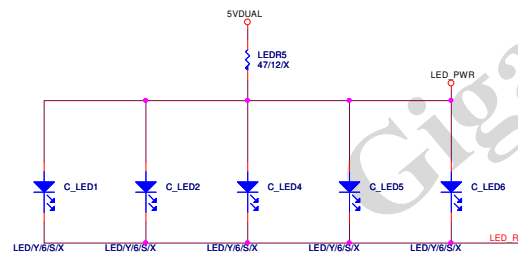
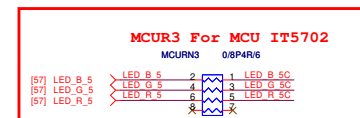
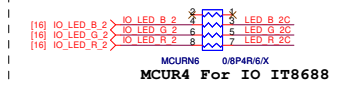
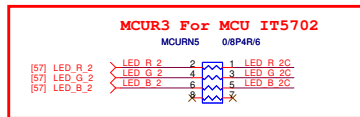
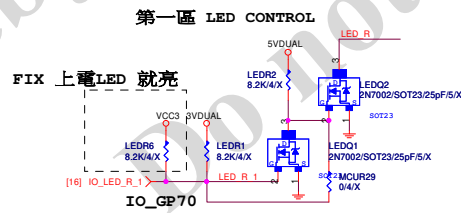
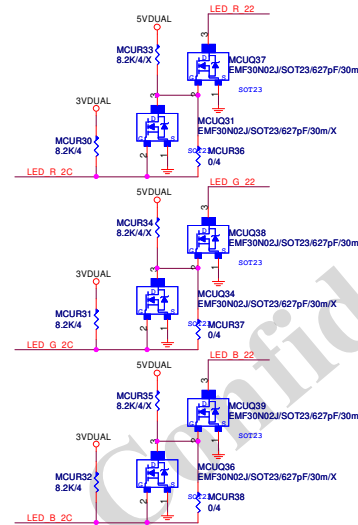
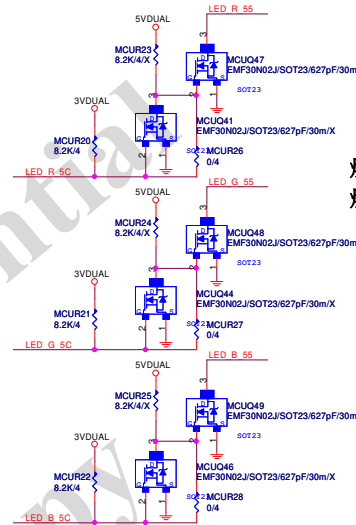
Q-Flash
Power Sequence

GPD0 pull-up to 3VSB
To ignore the test mode



Gigabyte Technology

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**B460M DS3H AC[N/A]****B460M DS3H AC[N/A]****第二區 LED CONTROL****第五區 LED CONTROL**

燈條 LED (LED_C1放在PCB左邊板邊位置)

燈條 LED (LED_C2放在PCB右邊板邊位置)

